Introduction to MSP430 Communication Interfaces

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Agenda

- USART, USCI, USI Comparison
- RS232 Communication
- SPI Communication
- I2C Communication
- Lab Activities

MSP430 Communication Modules

USART	USCI NEW	USI NEW
UART: - Only one modulator - n/a - n/a - n/a	**UART:** - Two modulators support n/16 timings - Auto baud rate detection - IrDA encoder & decoder - Simultaneous USCI_A and USCI_B (2 channels)	- - -
SPI: - Only one SPI available - Master and Slave Modes - 3 and 4 Wire Modes	**SPI:** - Two SPI (one on each USCI_A and USCI_B) - Master and Slave Modes - 3 and 4 Wire Modes	**SPI:** - Only one SPI available - Master and Slave Modes
I2C: *(on '15x/'16x only)* - Master and Slave Modes - up to 400kbps	**I2C:** - Simplified interrupt usage - Master and Slave Modes - up to 400kbps	**I2C:** - SW state machine needed - Master and Slave Modes

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- SPI Communication
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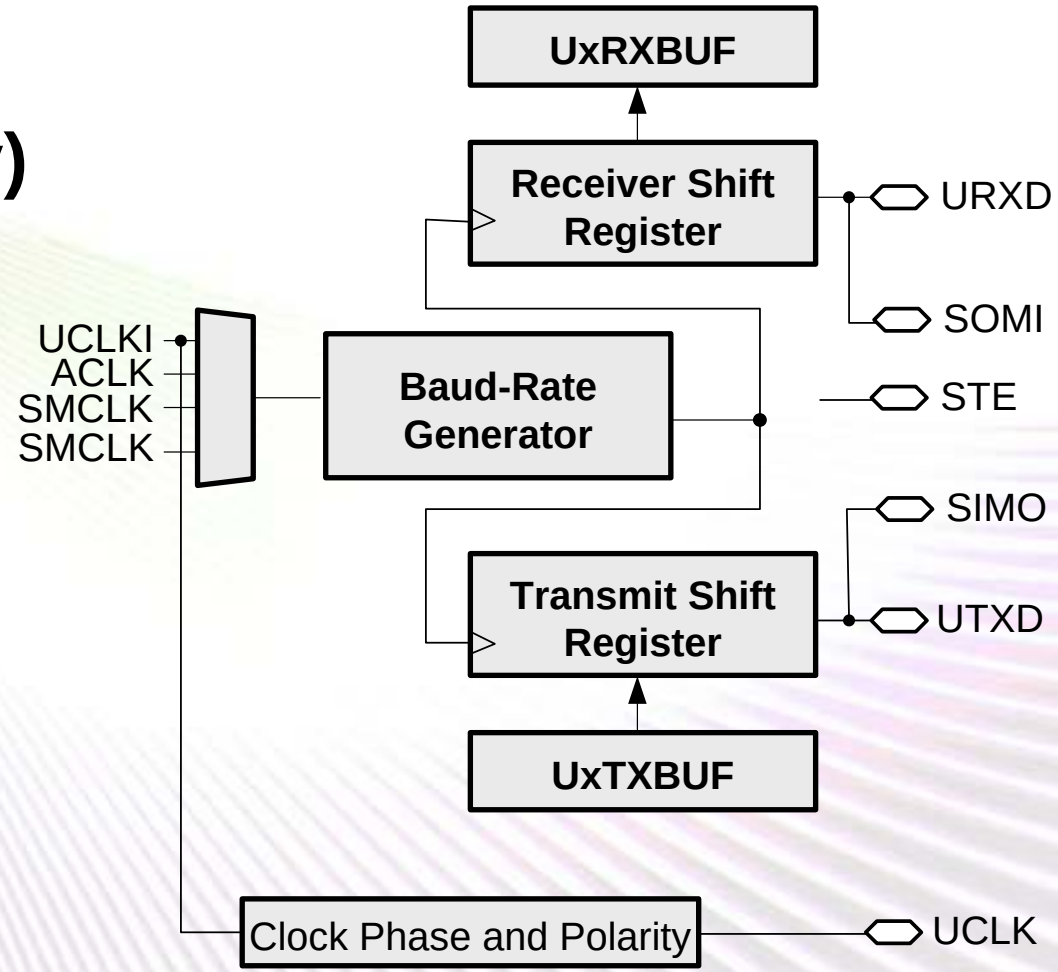
USART

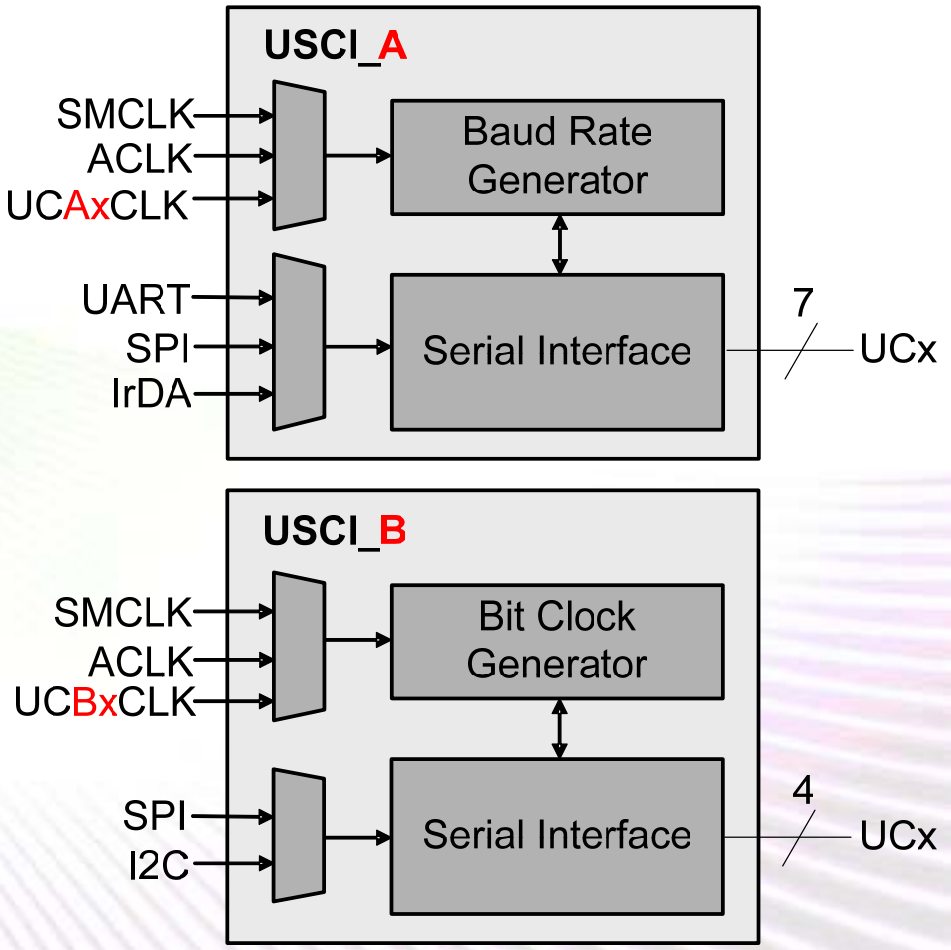
- **Ultra-Low Power Support:**
  - Auto-Start from any Low-Power Mode
- **UART or SPI Mode (I2C on ‘F15x/’F16x only)**
- **Double Buffered TX/RX**
- **Baudrate Generator**
- **DMA enabled**
- **Error Detection**



Universal Serial Communication I/F

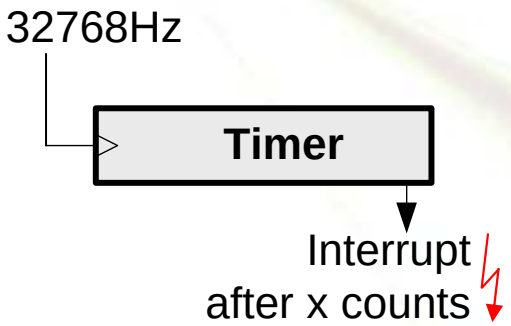
NEW

- **Ultra-Low Power Support:**
  - Auto-Start from any Low-Power Mode
- **Two Individual Blocks:**
  - USCI_A:
    UART with Lin/IrDA support
    SPI (Master/Slave, 3 & 4 wire mode)
  - USCI_B:
    SPI (Master/Slave, 3 & 4 wire mode)
    I2C (Master/Slave, up to 400kHz)
- **Double Buffered TX/RX**
- **Baudrate/Bit Clock Generator:**
  - With Auto-Baud Rate Detect
  - Flexible Clock Source
- **RX glitch suppression**
- **DMA enabled**
- **Error Detection**



RS232 Software Solution

- **Example:** 9600 Baud using 32.768kHz clock source

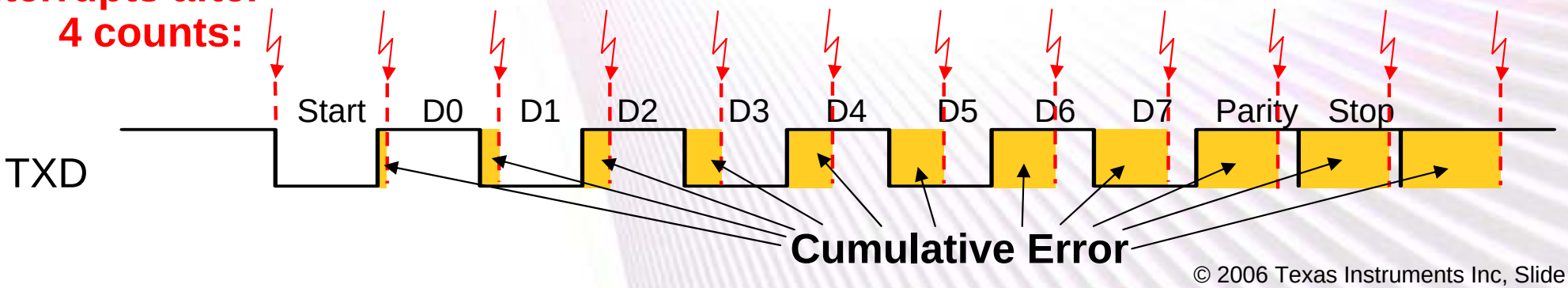



```
__interrupt void Timer_ISR()
{ if (Data & 0x01)  // check data bit 0
      SetOutput();  // bit0=1 → P1.0=1
  else
      ResetOutput();// bit0=0 → P1.0=0
  Data = Data >> 1; // next bit
}
```

9600 Baud ⇒ Bit Time = 104.17us ↔ **3x 32768Hz clocks = 91.55us**

4x 32768Hz clocks = 122.07us

Interrupts after 4 counts:



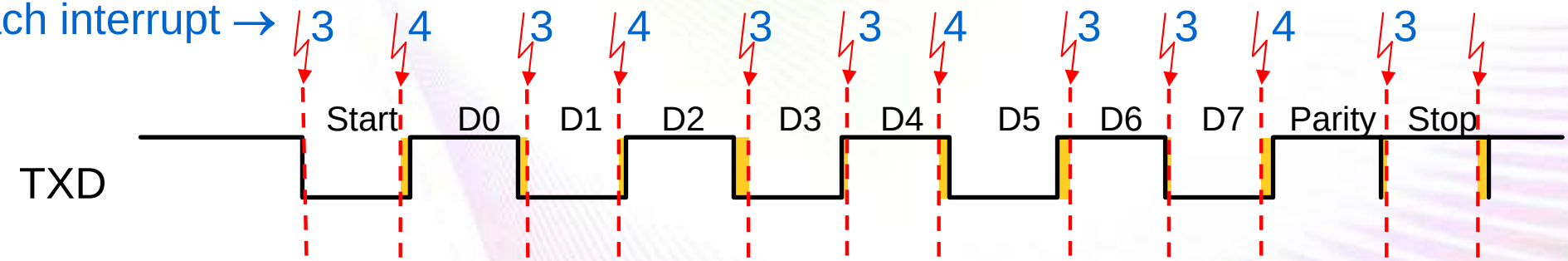
Reducing Cumulative Error

- **Modulation reduces Cumulative Error:**

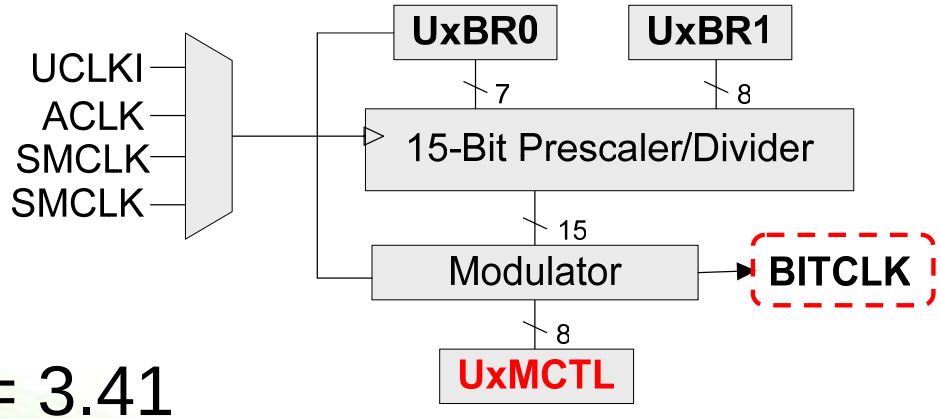
9600 Baud ⇒ Bit Time = 104.17us ↔ **3x 32768Hz clocks = 91.55us**

4x 32768Hz clocks = 122.07us

Redefine bit time
at each interrupt →



USART Baudrate Generator

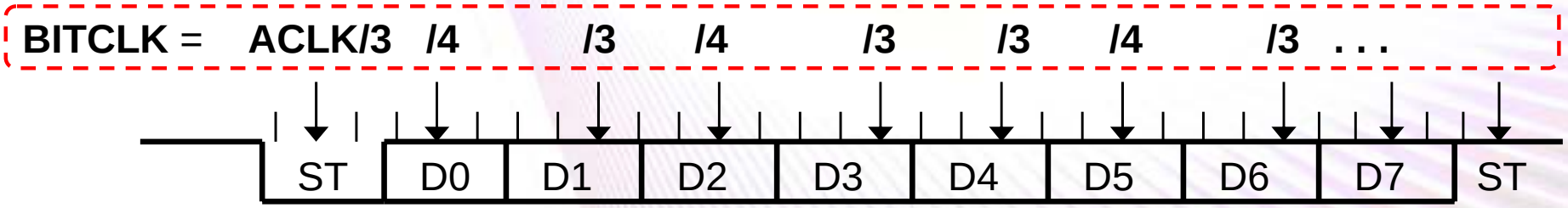


9600 baud:

ACLK = 32768 Hz

Prescaler = 32768Hz/9600baud = 3.41

UxBR1 | UxBR0 | UxMCTL = 00h | 03h | 4Ah

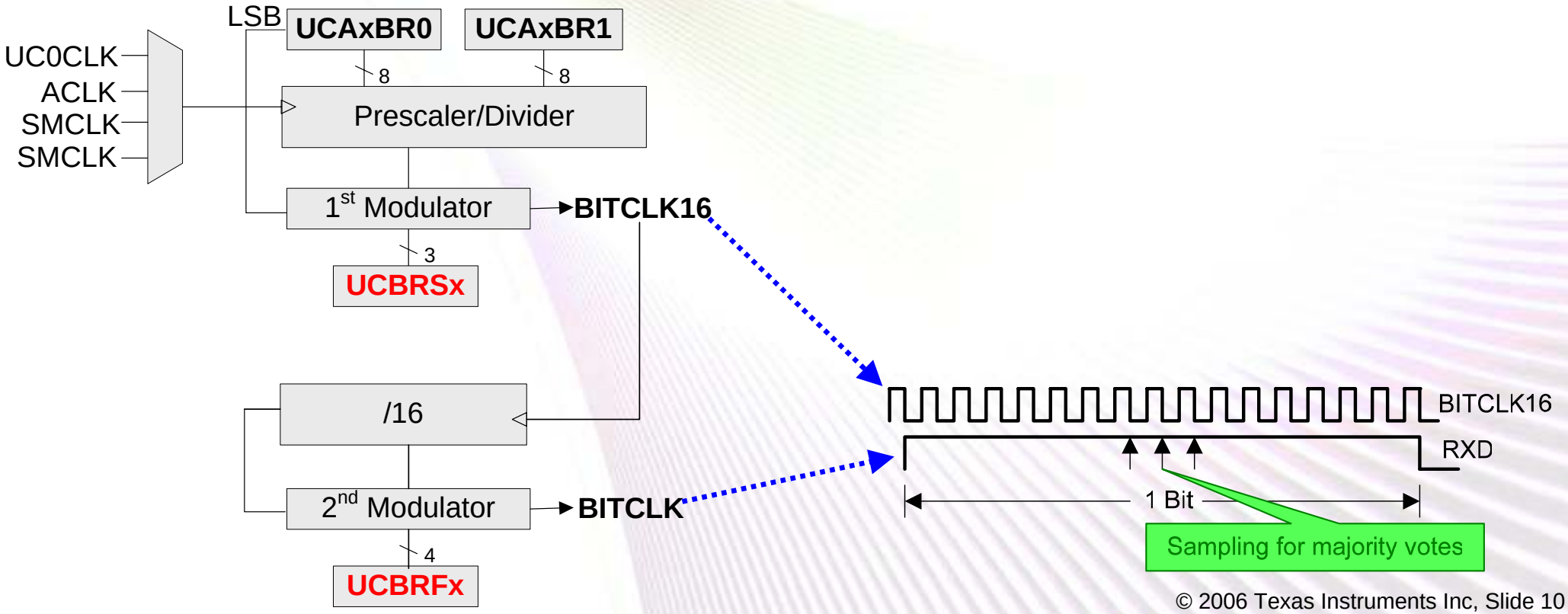


Content of UxMCTL is the modulation pattern

USCI Baudrate Generator

NEW

- **Oversampling Baud Rate Generation**
- **Two Modulators (UCBRSx and UCBRFx select modulation pattern)**
- **RX sampled using BITCLK16**



USART Initialization Sequence

Recommended USART initialization/re-configuration process as shown in the MSP430 User's Guide:

Note: Initializing or Re-Configuring the USART Module

The required USART initialization/re-configuration process is:

1) Set SWRST (`BIS.B #SWRST,&UxCTL`)

2) Initialize all USART registers with SWRST = 1 (including UxCTL)

3) Enable USART module via the MEx SFRs (URXEx and/or UTXEx)

4) Clear SWRST via software (`BIC.B #SWRST,&UxCTL`)

5) Enable interrupts (optional) via the IEx SFRs (URXIEx and/or UTXIEx)

Failure to follow this process may result in unpredictable USART behavior.

Please compare recommendations for USART Module in the MSP430 User's Guides.

USCI Initialization Sequence

Recommended USCI initialization/re-configuration process as shown in the MSP430 User's Guide:

Note: Initializing or Re-Configuring the USCI Module

The recommended USCI initialization/re-configuration process is:

1) Set UCSWRST (`BIS.B #UCSWRST,&UCAxCTL1`)
2) Initialize all USCI registers with UCSWRST = 1 (including UCAxCTL1)
3) Configure ports.
4) Clear UCSWRST via software (`BIC.B #UCSWRST,&UCAxCTL1`)
5) Enable interrupts (optional) via UCAxRXIE and/or UCAxTXIE

Please compare recommendations for USCI Module in the MSP430 User's Guides.

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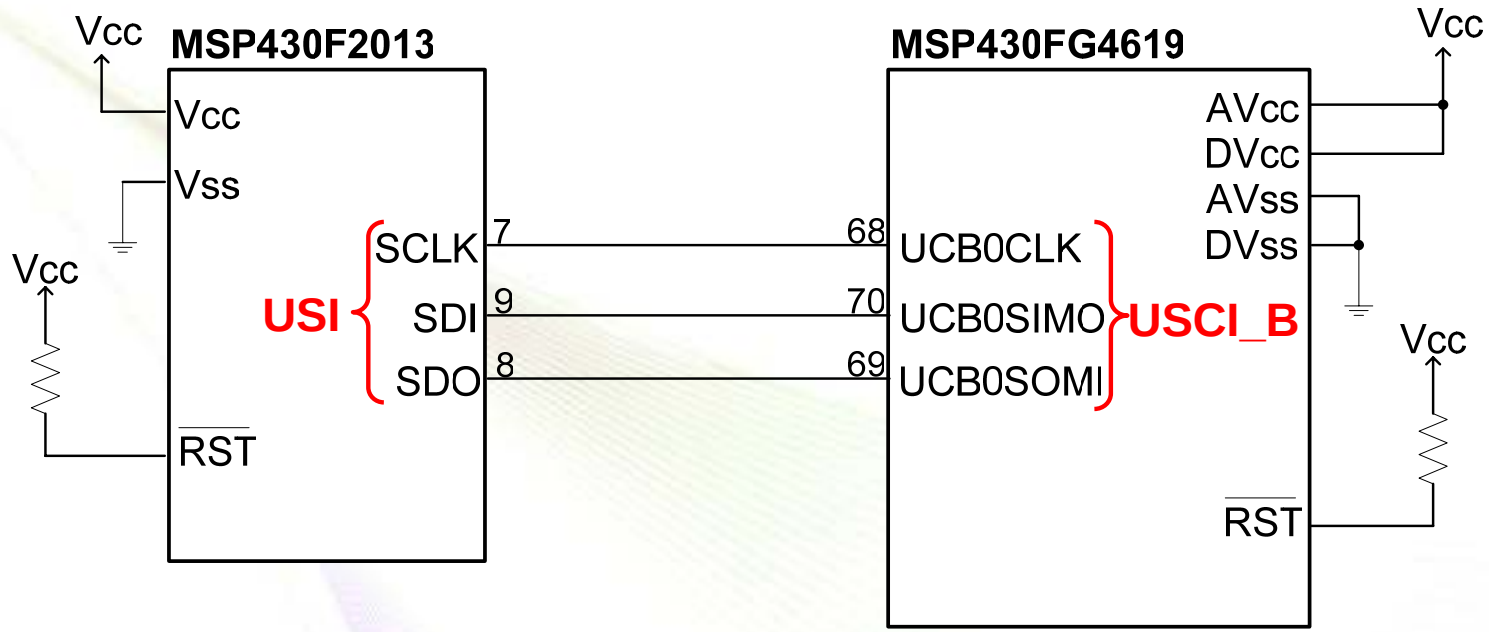
SPI Example

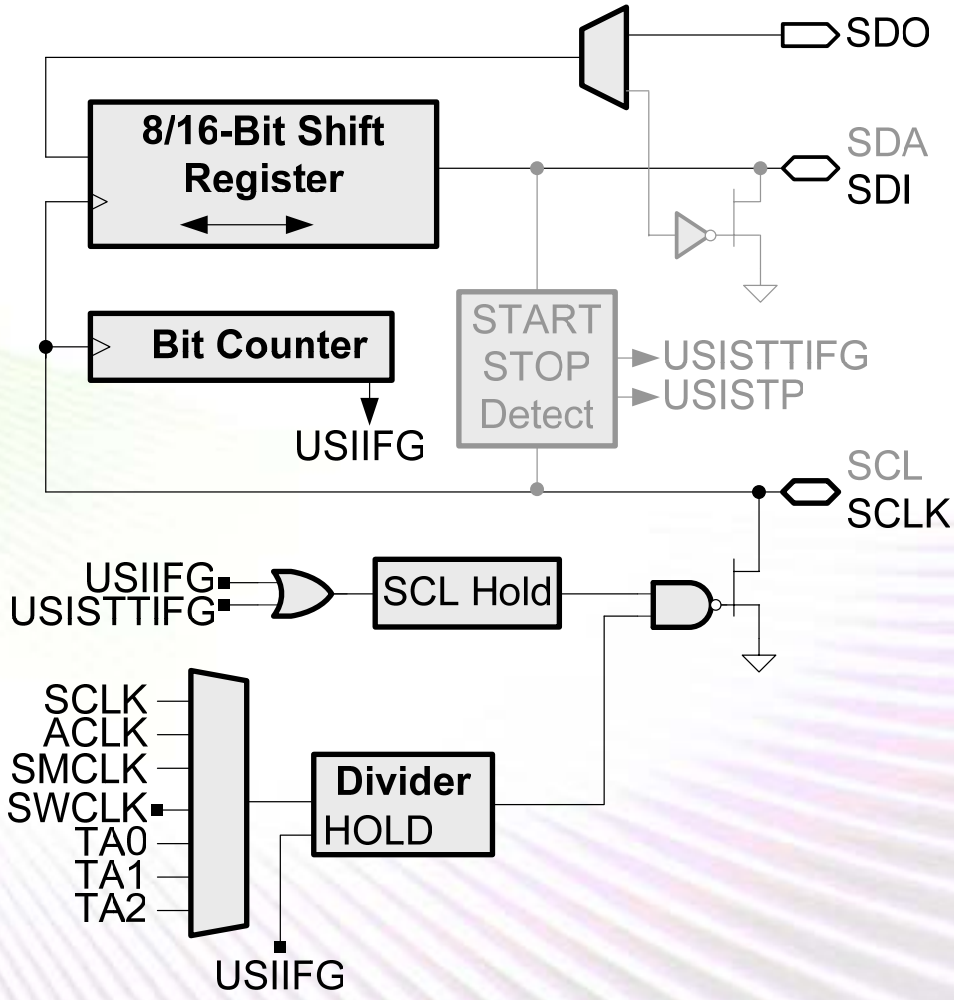


- **3 Wire Mode (MSP430 also supports 4-wire mode)**
- **Clock Phase and Polarity configurable**
- **Think about Start-up Behaviour**

Universal Serial Interface

NEW

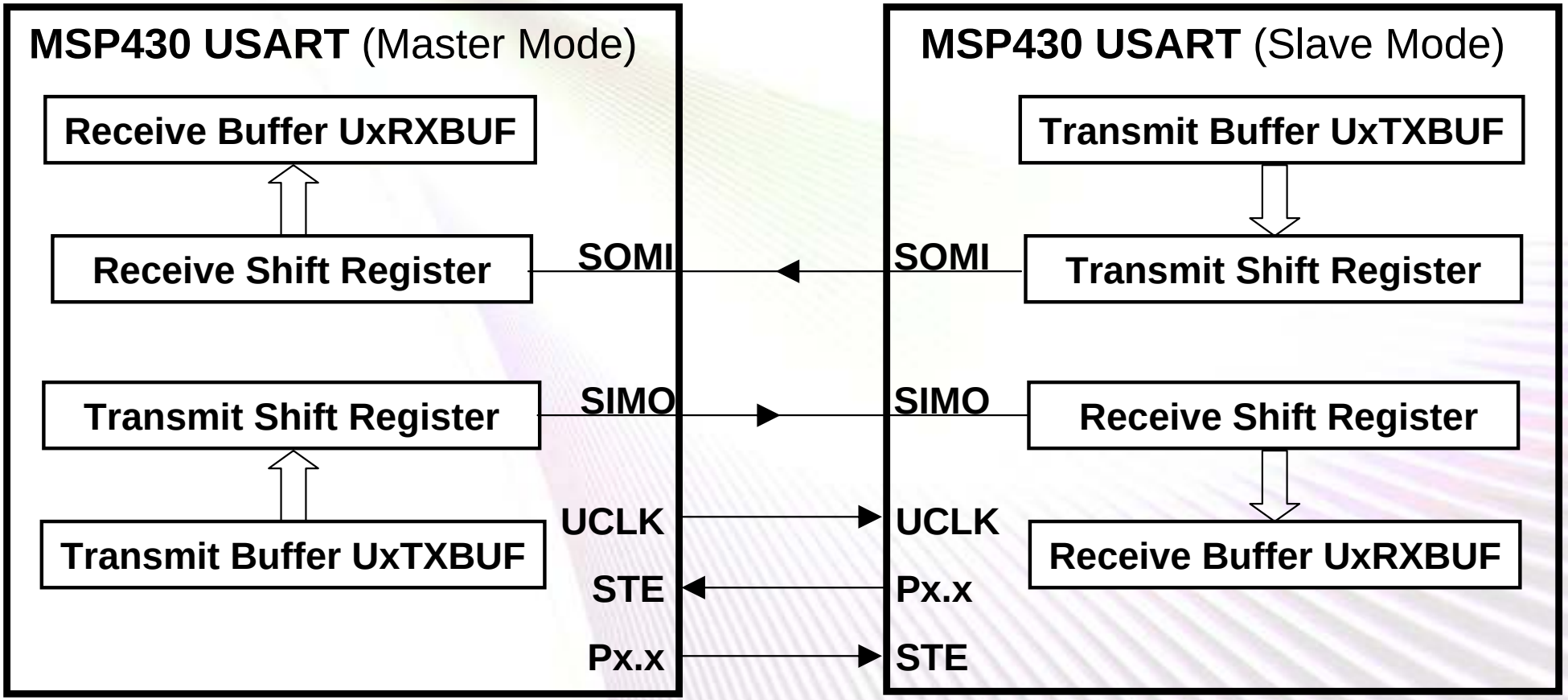
- Available on new MSP430x20xx family
- Supports I2C and SPI
- Programmable Data Length (up to 16-bits)
- Flexible Clock Source Selection



Provides efficient combination of cost & function for a software-friendly serial interface

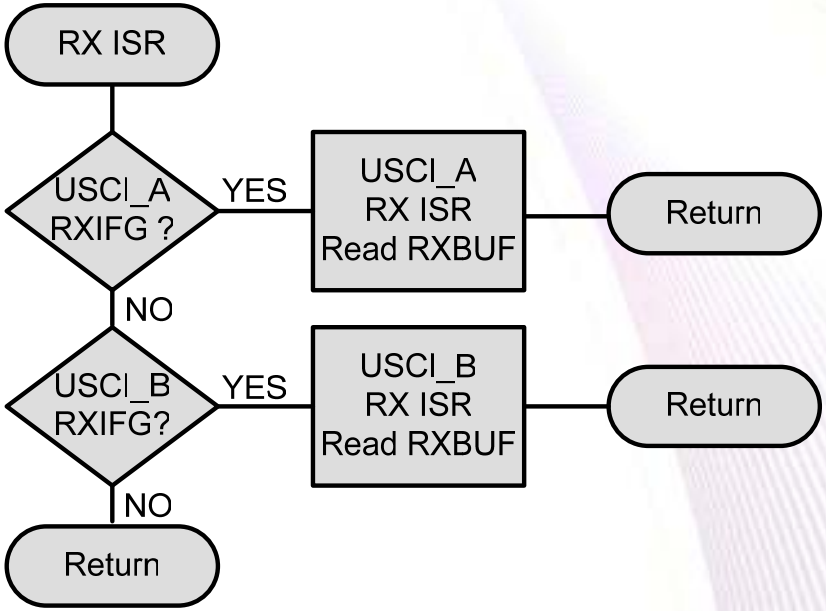
USART SPI

- **Supports Master and Slave Mode**
- **3-pin and 4-pin SPI operation**

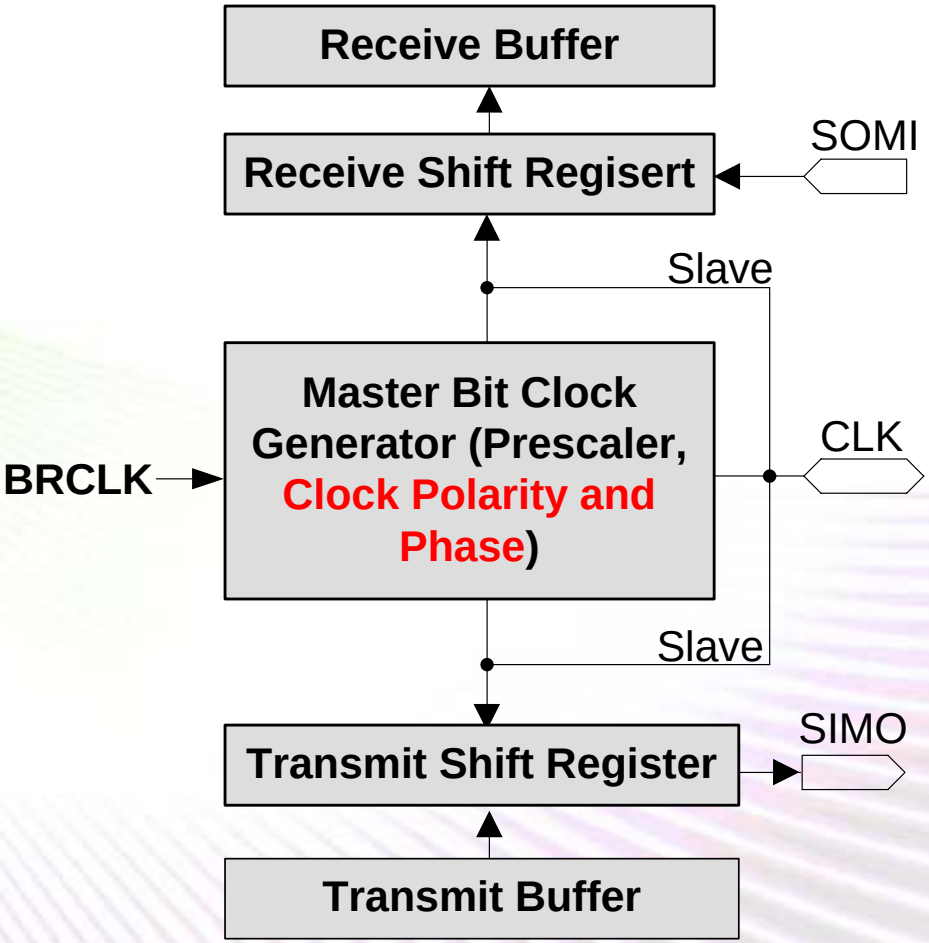


USCI: SPI Mode

- **Take care about Clock Polarity and Phase settings**
- **USCI_A and USCI_B share TX and RX vector**
- **Software check detects correct ISR handle:**



USCI SPI Block Diagram:



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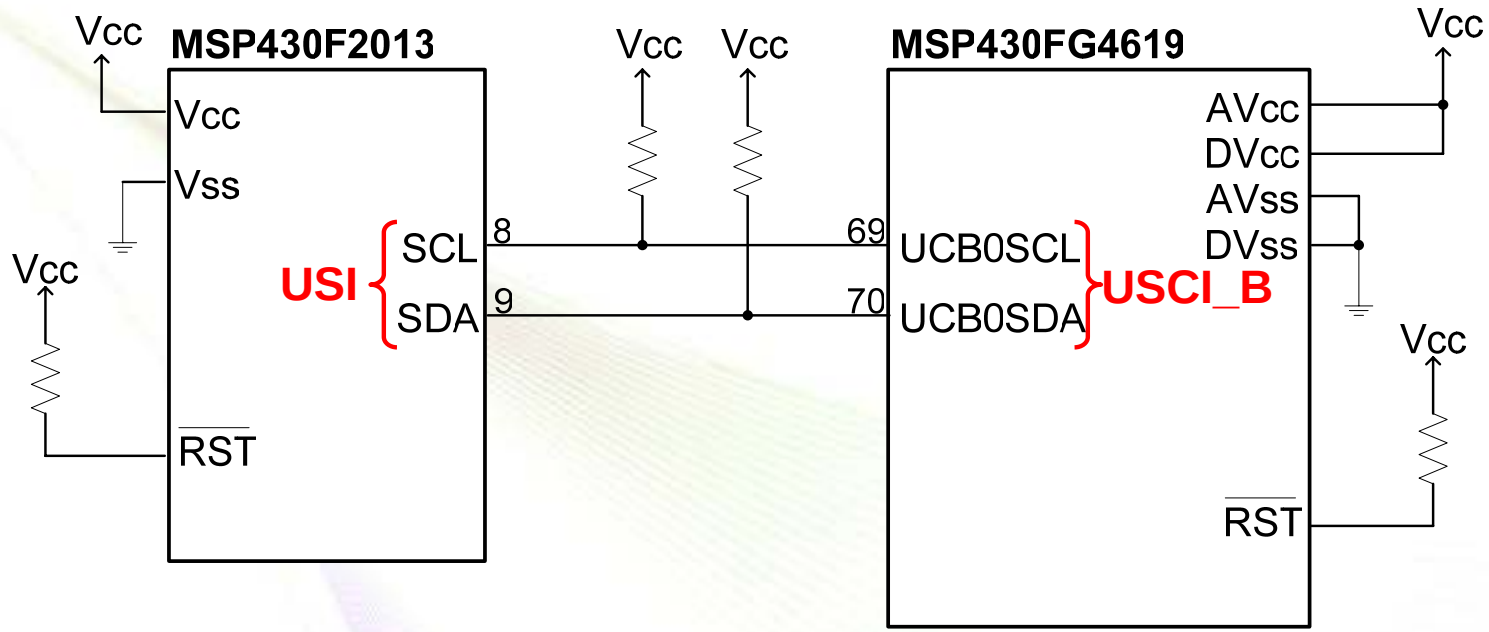
I2C-Bus Example

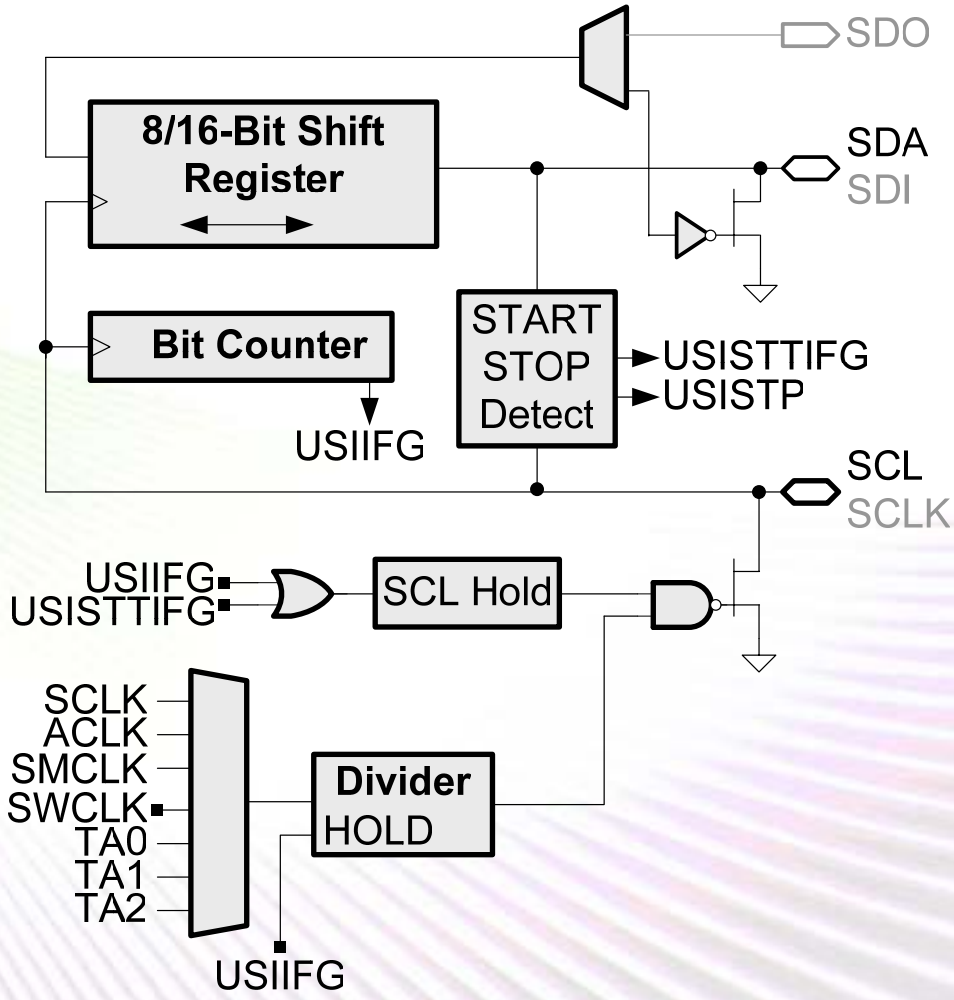


- **MSP430F2013:**
  - **USI I2C Slave Mode**
  - **Data (2 Bytes) are sent via I2C**
- **MSP430FG4619:**
  - **USCI I2C Master Mode**
  - **Data (2 Bytes) are read via I2C**

Universal Serial Interface

NEW

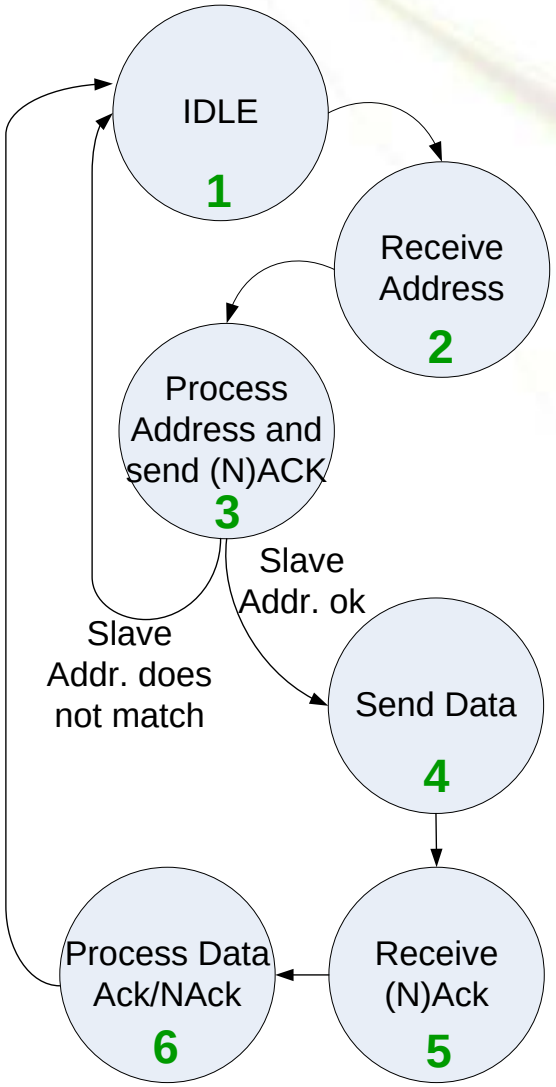
- Available on new MSP430x20xx family
- Supports I2C and SPI
- Programmable Data Length (up to 16-bits)
- Flexible Clock Source Selection



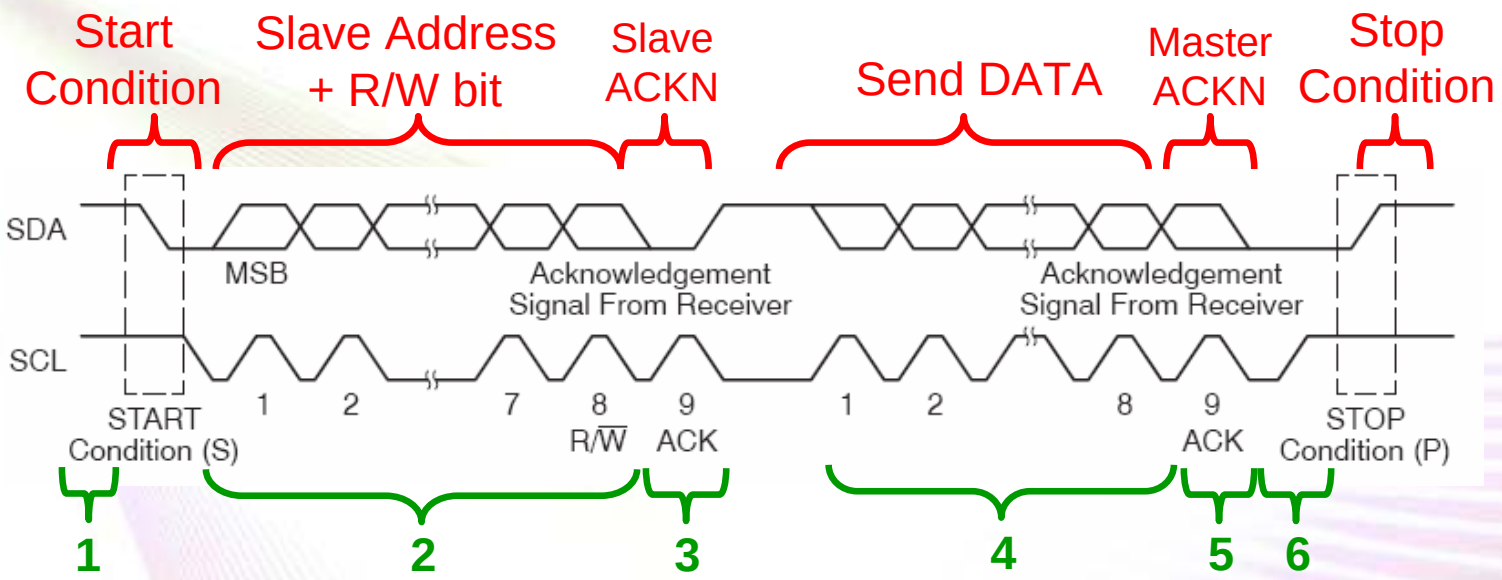
Provides efficient combination of cost & function for a software-friendly serial interface

USI: I2C Slave Transmitter

Software State Machine:

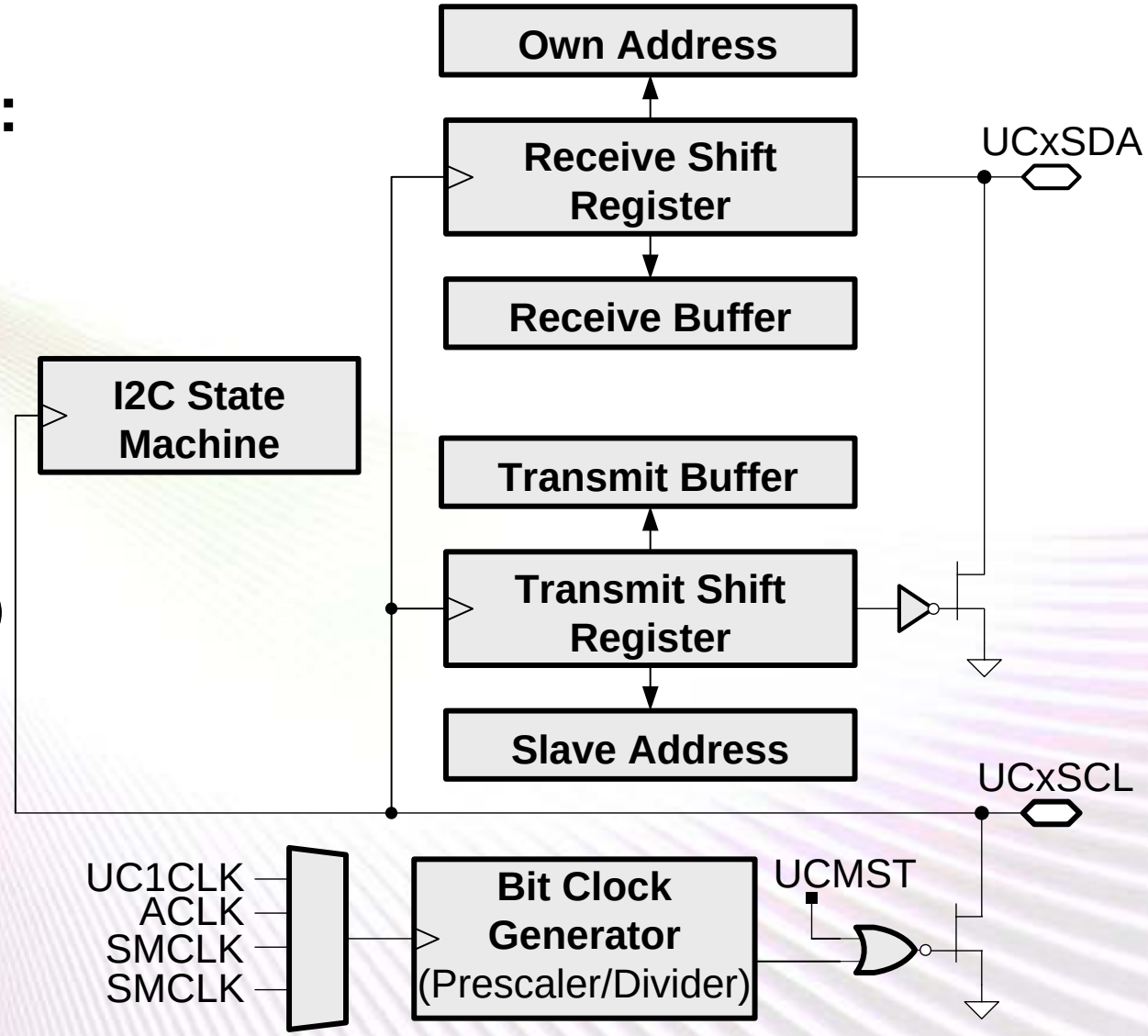


I2C Protocol:



USCI: I2C Communication

- **Compliance to I2C Specification V2.1:**
  - 7-bit/10-bit addressing
  - General call
  - Start/Restart/Stop
  - Multi-master transmitter/ receiver mode
  - Slave receiver/ transmitter mode
  - Standard mode (100kbps) and fast mode (400kbps) support
- **Flexible Bit Clock Generator**
- **Designed for Low Power**



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LAB 1: Instructions

- Start IAR Embedded Workbench and create a new Project
- Add the file "msp430xG46x_uscia0_uart_01_115k_modified.c" to the project
- Configure the project options (PROJECT → OPTIONS)
- Download the code and start the code
- Check RS232 communication between PC and your ATC board
  (The demo code will echo back received characters)
- You may change the baud rate by modifying the marked code lines on the following slide (more information about these control registers can be found on slide 26)

LAB 1: RS232 Communication

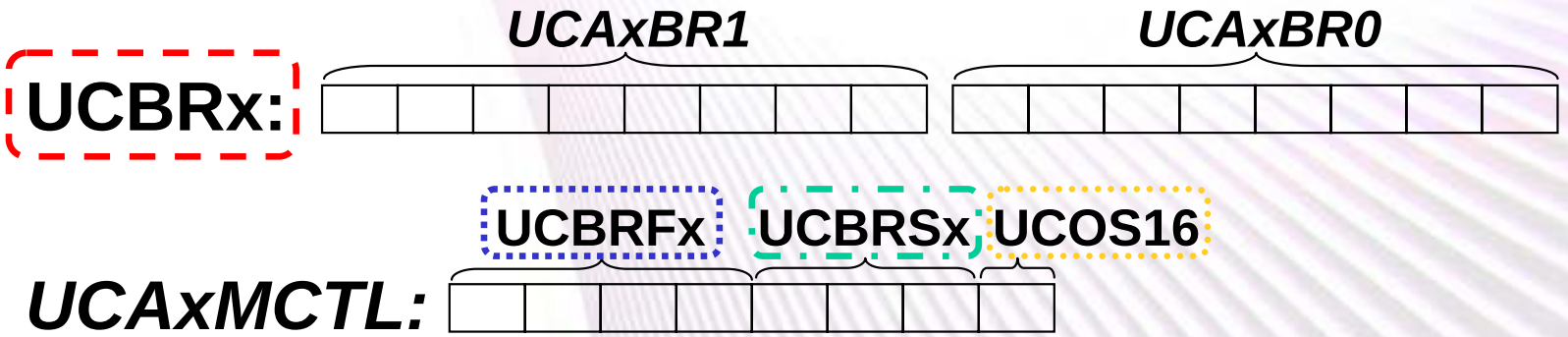
```
void main(void)    // FILE: “msp430xG46x_uscia0_uart_01_115k_modified.c”
{ WDTCTL = WDTPW+WDTHOLD;                 // Stop WDT
  FLL_CTL0 |= XCAP14PF;                   // Configure load caps
  //… check 32kHz oscillator
  P2SEL |= 0x030;                         // P2.4,5 = USCI_A0 RXD/TXD
  UCA0CTL1 |= UCSSEL_2;                   // SMCLK
  UCA0BR0 = 0x09;                         // 1MHz 115200
  UCA0BR1 = 0x00;                         // 1MHz 115200
  UCA0MCTL = 0x02;                        // Modulation
  UCA0CTL1 &= ~UCSWRST;     // **Initialize USCI state machine**
  IE2 |= UCA0RXIE;          // Enable USCI_A0 RX interrupt
  _BIS_SR(LPM0_bits + GIE); // Enter LPM0, interrupts enabled
}

//  Echo back RXed character, confirm TX buffer is ready first
#pragma vector=USCIAB0RX_VECTOR
__interrupt void USCIA0RX_ISR (void)
{ while(!(IFG2&UCA0TXIFG));
  UCA0TXBUF = UCA0RXBUF;                   // TX -> RXed character
}
```

LAB 1: Modify Baudrate

MSP430x4xx User's Guide/USCI Module Description:

Table 18–4. Commonly Used Baud Rates, Settings, and Errors, UCOS16 = 0

	BRCLK frequency [Hz]	Baud Rate [Baud]	UCBRx	UCBRSx	UCBRFx	Max. TX Error [%]		Max. RX Error [%]	
UCA0CTL1|= UCSSEL_1;	32,768	1200	27	2	0	–2.8	1.4	–5.9	2.0
	32,768	2400	13	6	0	–4.8	6.0	–9.7	8.3
	32,768	4800	6	7	0	–12.1	5.7	–13.4	19.0
	32,768	9600	3	3	0	–21.1	15.2	–44.3	21.3
UCA0CTL1|= UCSSEL_2;	1,048,576	9600	109	2	0	–0.2	0.7	–1.0	0.8
	1,048,576	19200	54	5	0	–1.1	1.0	–1.5	2.5
	1,048,576	38400	27	2	0	–2.8	1.4	–5.9	2.0
	1,048,576	56000	18	6	0	–3.9	1.1	–4.6	5.7
	1,048,576	115200	9	1	0	–1.1	10.7	–11.5	11.3



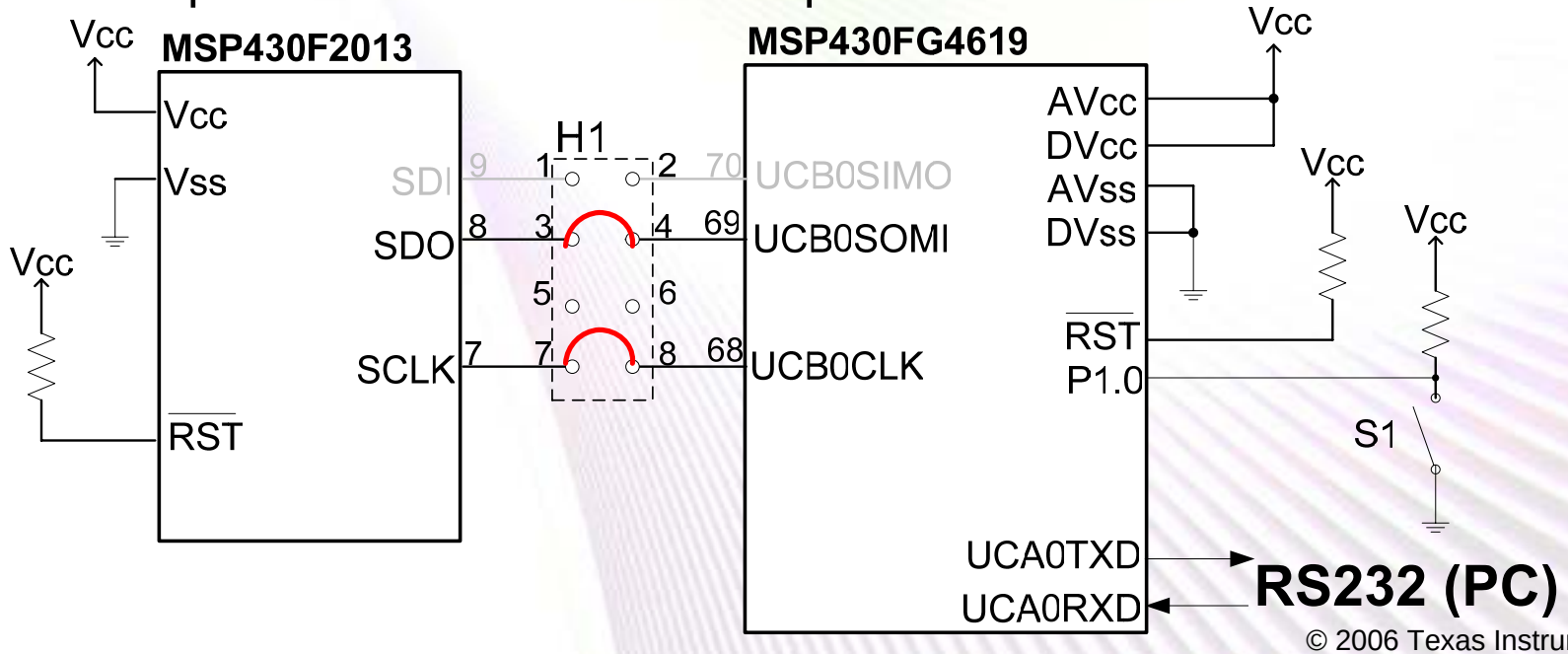
LAB 2: SPI with USI and USCI

1. MSP430F2013:

- Download code “msp430x20x3_usi_03_modified.c”

2. MSP430FG4619:

- Download code “msp430xG46x_uscib0_spi_01_modified.c”
- Check Jumper on connector H1 (3-4, 7-8)
- Connect RS232 (115kBaud, 8bit, no parity)
- Press push-button S1 to read sequence via SPI and show it on PC



LAB 2: Scope Shot of SPI & RS232

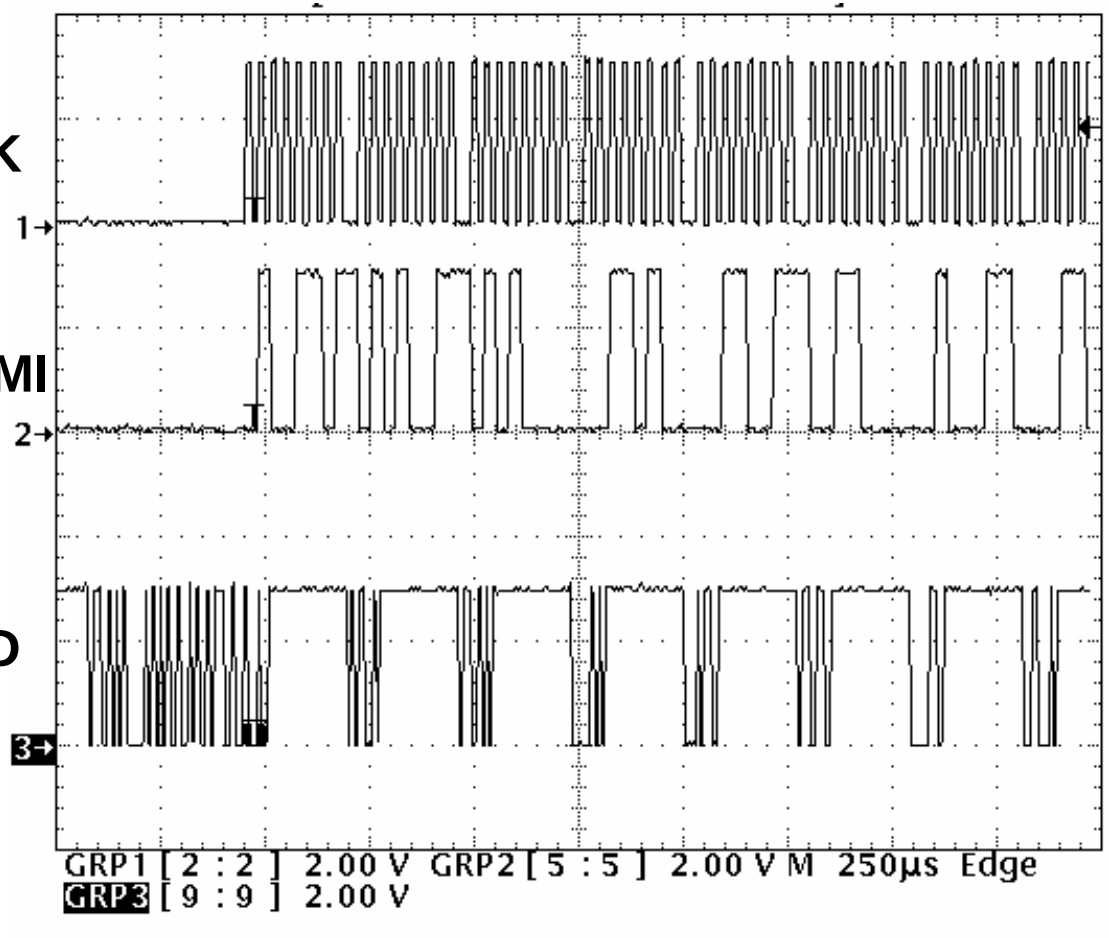
SPI Bus

UCB0CLK

UCB0SOMI

RS232

TXD



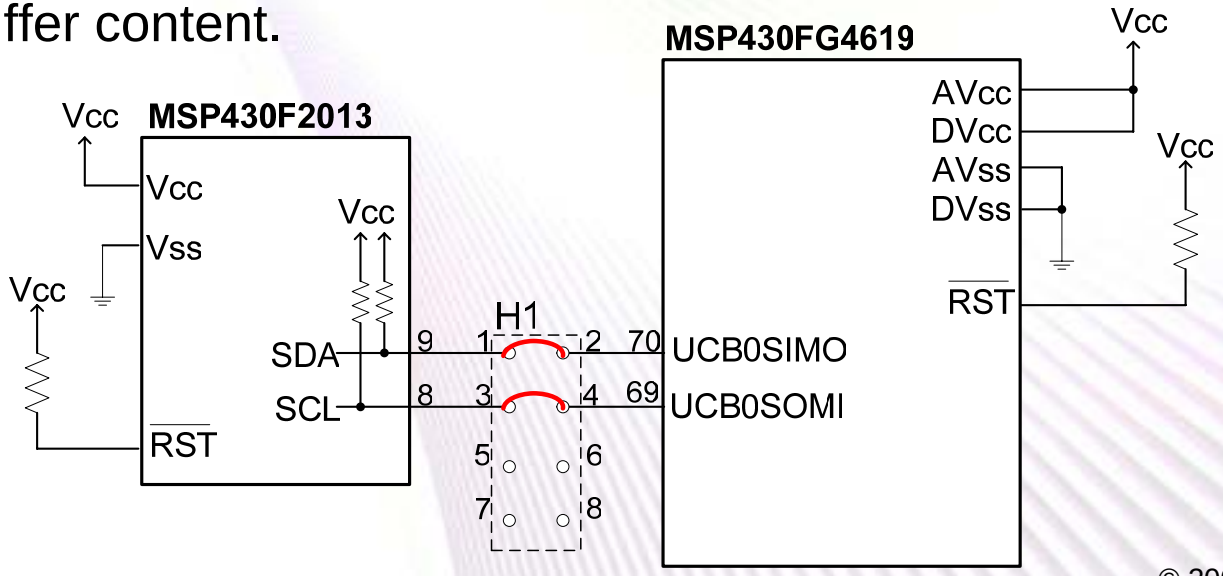
LAB 3: I2C with USI and USCI

1. MSP430F2013:

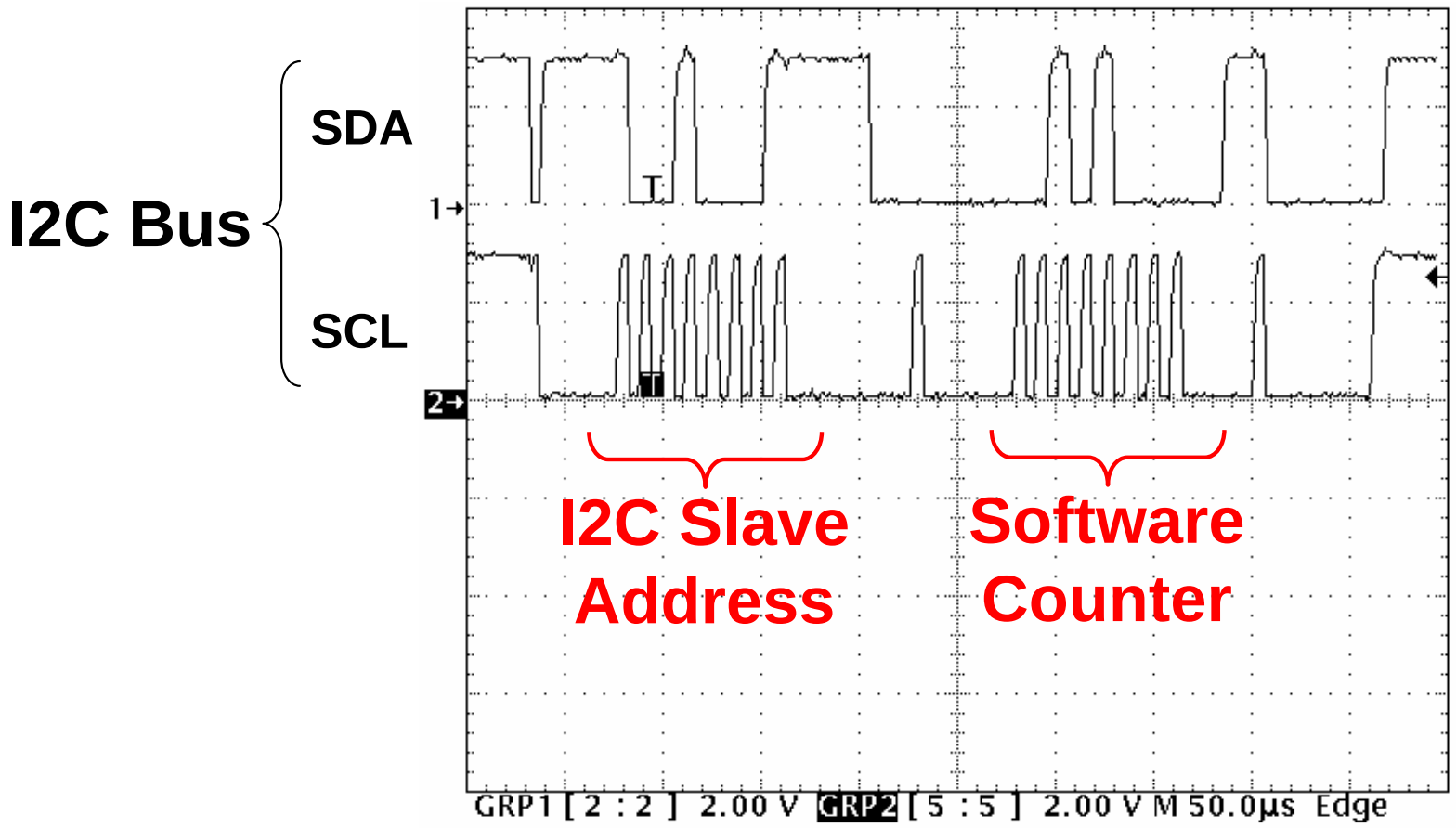
- Download code “msp430x20x3_usi_09_modified.c”

2. MSP430FG4619:

- Download code “msp430xG46x_uscib0_i2c_10_modified.c”
- Check Jumper on connector H1 (1-2, 3-4)
- Set breakpoint in main loop (look for comment “// Set BREAKPOINT >>here<<“)
- Start program execution. As soon as breakpoint was detected check RxBuffer content.



LAB 3: Scope Shot I2C Bus



Summary

- There are different solutions! MSP430's peripheral communication modules helps you to reduce CPU loading
- Be aware about the initialization sequence of USART and USCI modules (follow the recommendations of the User's Guides)
- Detailed module descriptions can be found in the MSP430 User's Guides
- Code examples are available on the MSP430 homepage (www.ti.com/msp430)

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