

# **R2010C**

**FAST ETHERNET RISC PROCESSOR**

**RDC** *RISC DSP Communication*

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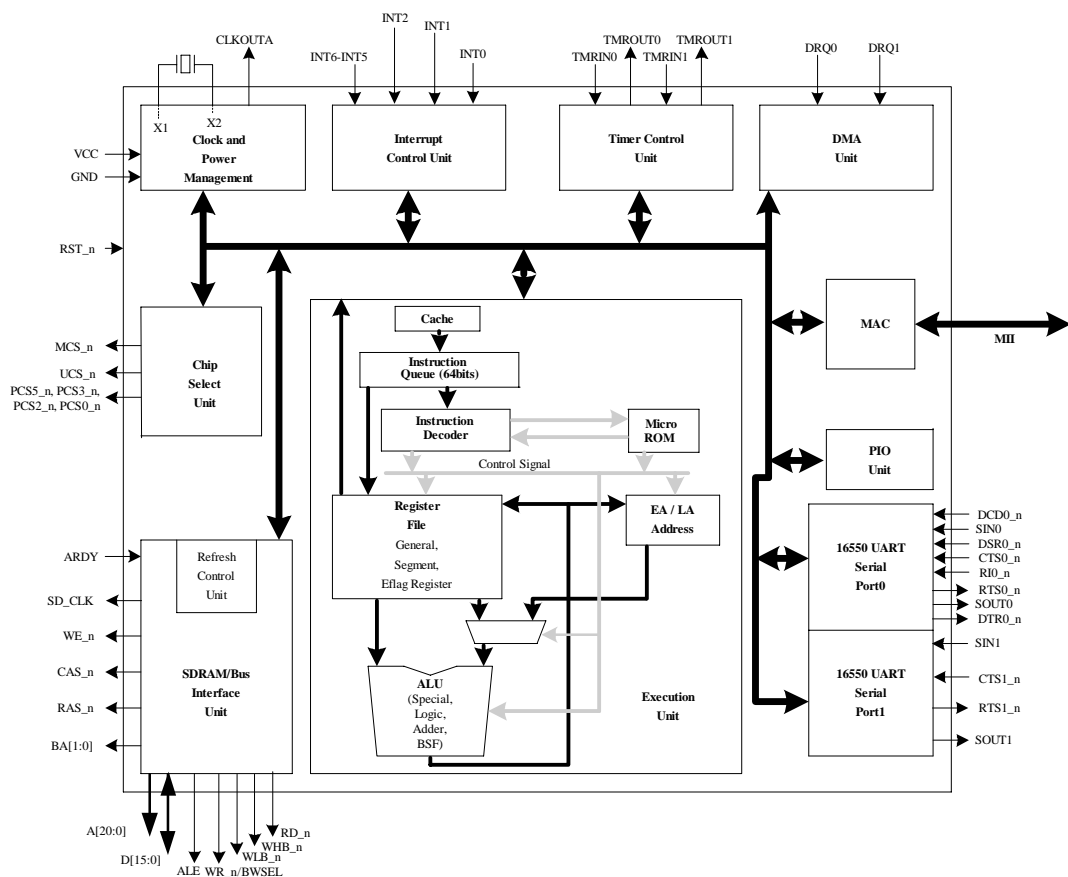
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## **1. Features**

- Five-stage pipeline
  - RISC architecture
  - Bus interface
    - Multiplexed address and Data bus
    - Supports non-multiplexed address bus A [20:0]
    - 16-bit external bus dynamic access
    - 16M-byte memory address space
    - 64K-byte I/O space
    - Supports an independent data/address bus for external I/O device
    - Supports a glueless and simplified 16-bit PCMCIA bus interface
  - Supports two compatible UART serial channels with 16-byte FIFO and hardware flow-control.
  - Supports CPU ID
  - SDRAM control Interface
  - Three independent 16-bit timers and one independent programmable watchdog timer
  - The Interrupt controller with five maskable external interrupts
  - Two independent DMA channels
  - Programmable chip-select logic for Memory or I/O bus cycle decoder
  - Programmable wait-state generator
  - With 8-bit or 16-bit Boot ROM bus size
  - 1-Port Fast Ethernet MAC with MII interface
  - Supports an 8K-byte Uniform cache
  - With 25MHz input frequency and up to 100MHz maximum internal frequency.
  - Compatible with 3.3V I/O and 2.5V core voltage.
  - Package Type includes 128-pin PQFP.
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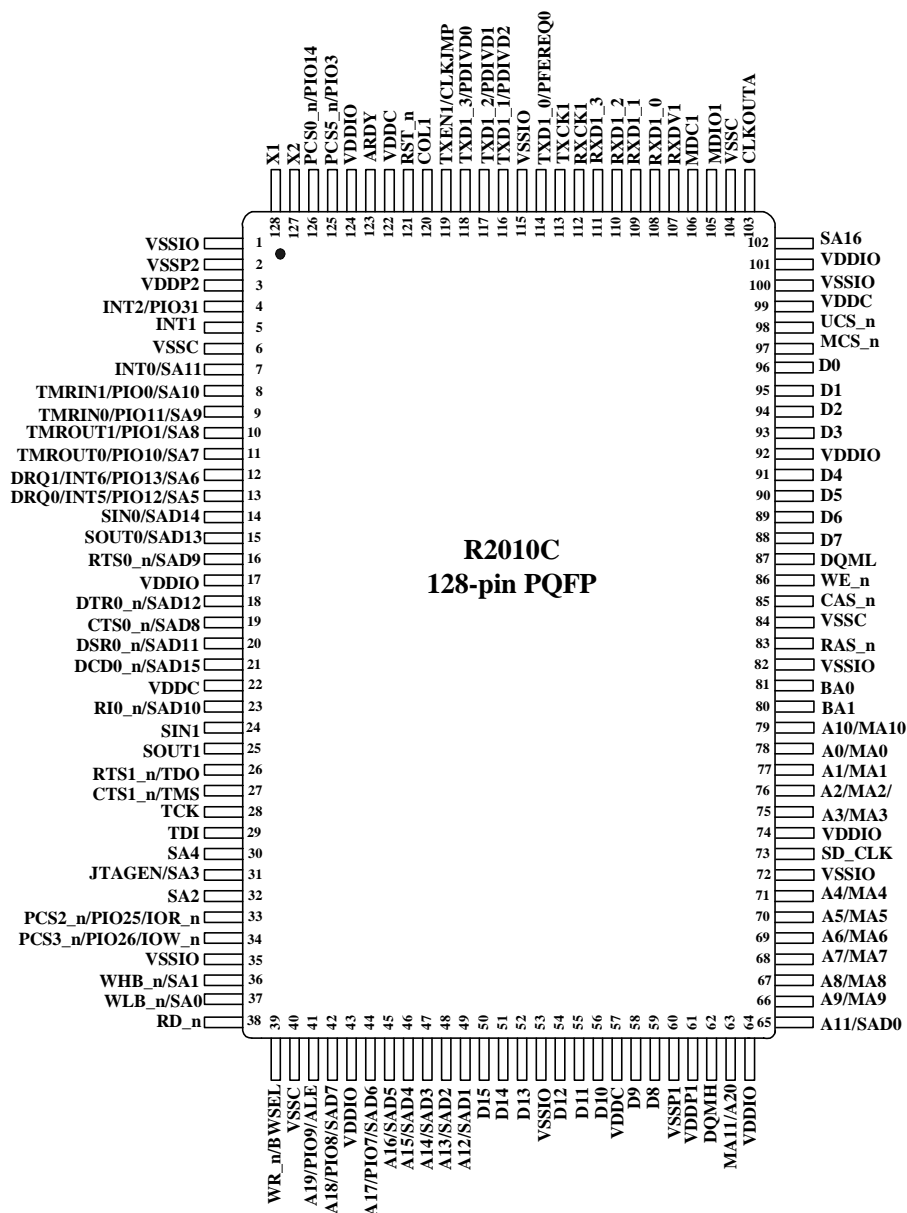
## 2. Block Diagram





### 3. Pin Description

#### 3.1 Pin Placement



### 3.2 Functional Description

I = Input;

O = Output;

PU = Pull up 75K ;

PD = Pull down 75K ;

PU\* = Pull up 75K when the PION pin is used;

PD\* = Pull down 75K when the PION pin is used;

#### CPU Core

PIN No.	Symbol	Type	Description
121	RST_n	I/PU	Reset input with Schmitt trigger. When RST_n is asserted, the CPU immediately terminates all operations, clears the internal registers & logic, and changes the address to the reset address FFFF00h.
128	X1	I	25MHz frequency input, <u>within 100 ppm tolerance</u> , to the amplifier (oscillator).
127	X2	O	Frequency output from the inverting amplifier (oscillator).
103	CLKOUTA	O	The CLKOUTA output frequency is the same as the X1 input frequency. When high, the CLKOUTA is from Multiple-PLL. When low, the CLKOUTA is from X1.

#### Bus Interface

PIN No.	Symbol	Type	Description
36	WHB_n/SA1	O	Write high byte. This pin indicates that the high byte data (D[15:8]) on the bus is to be written to a memory or an I/O device. This pin floats during reset or bus hold conditions. SA1: The slow bus address 1
37	WLB_n/SA0	O/PU	Write low byte. This pin indicates that the low byte data (D[7:0]) on the bus is to be written to a memory or an I/O device. This pin floats during reset or bus hold conditions. <b>This pin must be pulled low.</b> SA0: The slow bus address 0
38	RD_n	O	Read Strobe. One active low signal indicates that the microcontroller is performing a memory or I/O read cycle. The RD_n floats during a bus hold or reset.
39	WR_n/BWSEL	O/PU	Write strobe. This pin indicates that the data on the bus is to be written into a memory or an I/O device. WR_n is active during T2, T3, and Tw of any write cycle, floating during a bus hold or reset. BWSEL is used to decide the boot ROM bus width when RST_n goes from low to high.

			If BWSEL is with an external pull-low resistor (4.7k ohm), the boot ROM bus width is 8 bits. Otherwise the boot ROM width is 16 bits.
123	ARDY	I/PU	Asynchronous ready. This pin indicates to the microcontroller that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge of input that is asynchronous to SD_CLK and is active high. However, the falling edge of ARDY must be synchronized to SD_CLK. Tie ARDY high, so the microcontroller is always asserted in the ready condition. To guarantee the wait states inserted, ARDY must be pulled low before to phase 2 of T2 or phase 1 of T3. Please note that the ARDY signal is internally pulled high.
41 42 44 45 46 47 48 49 65 79 66 67 68 69 70 71 75 76 77 78	A19/PIO9/ALE A18/PIO8/SAD7 A17/PIO7/SAD6 A16/SAD5 A15/SAD4 A14/SAD3 A13/SAD2 A12/SAD1 A11/SAD0 A10/MA10 A9/MA9 A8/MA8 A7/MA7 A6/MA6 A5/MA5 A4/MA4 A3/MA3 A2/MA2 A1/MA1 A0/MA0	I/O	Address bus. Non-multiplexed memory or I/O addresses. The address bus is one-half of a SD_CLK period earlier than the D bus. The address bus is in a high-impedance state during a bus hold or reset.  SAD [7:0]: The combination pins with addresses and data. They are designed for slower peripheral bus.  ALE: Address latch enable. Active high. This pin indicates an address output on the D bus. Address is guaranteed to be valid on the trailing edge of ALE. This pin is three-stated during ONCE mode and never floats during bus hold or reset conditions.  MA [10:0]: The SDRAM row and column address output.
96 95 94 93 91 90 89 88 59 58 56 55 54	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12	I/O	The data bus for memory or I/O accesses. The data bus phase is in t2-t4 cycle.  The D bus is in a floating state during a bus hold or reset condition and this bus can also be used to load system configuration information (with pull-up or pull-low resistor) into the RESCON register when RST_n goes from low to high and the Watchdog timeout is reset.

52	D13		
51	D14		
50	D15		
32	SA2	O/PD	SA4: The slow bus address 2
30	SA4	I/O/PU	SA4: The slow bus address 4
102	SA16	I/O/PD	SA16: The slow bus address 16

**Chip Select Unit Interface**

PIN No.	Symbol	Type	Description
98	UCS_n	I/O/PU	Upper memory chip select. For UCS_n, this pin is active low when the system accesses the defined portion of the upper 8M bytes (800000-FFFFFF) memory block. UCS_n defaulted active address region is from FF0000h to FFFFFFFh after power-on reset. The address range for UCS_n is programmed by software. This pin incorporates a weak pull-up resistor.
97	MCS_n	O/PU	Midrange Memory Chip Select For MCS_n feature, this pin is active low when the microcontroller accesses the defined portion of memory region.
125	PCS5_n/PIO3	I/O/PU*	Peripheral chip selects/latched address bit. For PCS_n feature, these pins are active low when the micro-controller accesses the fifth or sixth region of the peripheral memory (I/O or memory space). The base address of PCS_n is programmable. These pins are asserted with the multiplexed D address bus and do not float during bus hold conditions.
126	PCS0_n/PIO14	I/O/PU*	Peripheral chip selects. These pins are active low when the microcontroller accesses the defined peripheral memory block (I/O or memory address). For I/O access, the base address can be programmed in the region from 00000h to 0FFFFh. For memory address access, the base address can be located in the 16M-Byte memory address region. These pins assert with the multiplexed D address bus and do not float during bus holds.
33 34	PCS2_n/PIO25/IOR_n PCS3_n/PIO26/IOW_n	I/O/PU*	Peripheral chip selects. These pins are active low when the micro controller accesses the defined peripheral memory block (I/O or memory address). For I/O access, the base address can be programmed in the region from 00000h to 0FFFFh. For memory address access, the base address can be located in the 16M-Byte memory address region. These pins assert with the multiplexed D address bus and do not float during bus holds. When register FFEAh bit is set, PIN36 is IOR_n and PIN37 is IOW_n. IOR_n/IOW_n are for PCMCIA bus.

**Interrupt Control Unit Interface**

PIN No.	Symbol	Type	Description
4	INT2/PIO31	I/O/PU*	Maskable Interrupt Request 2. It's active high. The interrupt input can be configured to be either edge-triggered or level-triggered. The requesting device must hold the INT2 until the request is acknowledged to

			guarantee interrupt recognition.
5	INT1	I/PD	Mask able Interrupt Request 1/slave select. Except the differences of the interrupt line and interrupt address vector, the function of INT1 is the same as that of INT2.
7	INT0/SA11	I/PD	Mask able interrupt request 0. Except the differences of the interrupt line and interrupt address vector, the function of INT0 is the same as that of INT2. SA11: The slow bus address 11

#### Timer Control Unit Interface

PIN No.	Symbol	Type	Description
8 9	TMRIN1/PIO0/SA10 TMRIN0/PIO11/SA9	I/O/PU*	Timer input. These pins can be used as clock or control signal input, depending upon the programmed timer mode. After internally synchronizing low to high transitions on TMRIN, the timer controller increments. <b>These pins must be pulled up if not being used.</b> SA[10:9]: The slow bus address 10 and 9
10 11	TMROUT1/PIO1/SA8 TMROUT0/PIO10/SA7	I/O/PD*	Timer output. Depending on timer mode select. These pins provide single pulse or continuous waveform. The duty cycle of the waveform is programmable. These pins are floated during a bus hold or reset. SA[8:7]: The slow bus address 8 and 7

#### DMA Unit Interface

12 13	DRQ1/INT6/PIO13/SA6 DRQ0/INT5/PIO12/SA5	I/O/PU*	DMA request. These pins are asserted high by an external device when the device is ready for DMA channel 1 or channel 0 to perform a transfer. These pins are level-triggered and internally synchronized. The DRQ signals are not latched and must remain active until serviced. For INT6/INT5: When the DMA function is not used, the INT6 and INT5 can be used as an additional external interrupt request. And they share the corresponding interrupt type and register control bits. The INT6/5 are level-triggered only. SA[6:5]: The slow bus address 6 and 5
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#### 16550 UART

PIN No.	Symbol	Type	Description
14	SIN0/SAD14	I/O/PU	SIN0: Serial Input. Serial Data Input from the communications link. SAD14: The combination pin with Address and Data. It is for slower device bus.
15	SOUT0/SAD13	I/O/PU	SOUT0: Serial Output. Composite serial data output to the communications link. SAD13: The combination pin with Address and Data. It is for slower device bus.
16	RTS0_n/SAD9	I/O/PU	RTS0_n: Request To Send. When low, this indicates to MODEM or data set that URAT is ready to exchange data.

			SAD9: The combination pin with Address and Data. It is for slower device bus.
18	DTR0_n/SAD12	I/O/PU	DTR0_n: Data Terminal Ready. When low, this informs the MODEM or data set that UART is ready to establish a communication link. SAD12: The combination pin with Address and Data. It is for slower device bus.
19	CTS0_n/SAD8	I/O/PU	CTS0_n: Clear To Send. When low, this indicates to UART that MODEM or data set is ready to exchange data. SAD8: The combination pin with Address and Data. It is for slower device bus.
20	DSR0_n/SAD11	I/O/PU	DSR0_n: Data Set Ready. When low, this indicates that MODEM or data set is ready to establish the communication link with UART. SAD11: The combination pin with Address and Data. It is for slower device bus.
21	DCD0_n/SAD15	I/O/PU	DCD0_n: Data Carry Detection. When low, it indicates that the data carrier has been detected by the MODEM or data set. SAD15: The combination pin with Address and Data. It is for slower device bus.
23	RI0_n /SAD10	I/O/PU	RI0_n: Ring Indicator. This indicates that a telephone-ringing signal has been received by the MODEM or data set. SAD10: The combination pin with Address and Data. It is for slower device bus.
24	SIN1	I	SIN1: Serial Data Input.
25	SOUT1	O	SOUT1: Serial Data Output. <b>This pin must be pulled low.</b>
26	RTS1_n/TDO	O	RTS1_n: Request To Send. TDO: JTAG test data output pin.
27	CTS1_n/TMS	I/PU	CTS1_n: Clear To Send. JTAG Test mode select pin
28	TCK	I/PU	TCK: JTAG test clock input pin
29	TDI	I/PU	TDI: JTAG test data input pin

## MII Interface

PIN No.	Symbol	Type	Description
118 114	TXD1_3/PDIVD0 TXD1_0/PFREQ0	I/O/PU	Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal.
117 116	TXD1_2/PDIVD1 TXD1_1/PDIVD2	I/O/PD	PDIVD [2:0] & PFREQ [0] are hardware configured pins during reset for Multiple PLL. (See Chapter.5) PDIVD [2:0]: Multiple selections. PFREQ [0]: Input clock range selection.
119	TXEN1/CLKJMP	I/O/PD	This pin functions as transmit enable. It indicates that a transmission is active on the MII port to an external PHY

			device. CLKJMP: It is a hardware-configured pin, used to select the CLKOUTA output from internal Multiple PLL or X1. When high, the CLKOUTA is from Multiple-PLL. When low, the CLKOUTA is from X1.
113	TXC1	I/PD	Supports the transmit clock supplied by the external PMD device. This clock should always be active.
112	RXC1	I/PD	Supports the receive clock supplied by the external PMD device. This clock should always be active.
111 110 109 108	RXD1_3 RXD1_2 RXD1_1 RXD1_0	I/PD	Four parallel receive data lines. This data is driven by an external PHY that the media is attached and should be synchronized with the RXC signal.
107	RXDV1	I/PD	Data valid is asserted by an external PHY when the received data is present on the RXD1 [3:0] lines and is de-asserted at the end of the packet.
120	COL1	I/PD	This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin.
106	MDC1	O	MII management data clock is sourced by the R2010C to the external PHY devices as a timing reference for the information transfer on the MDIO signal.
105	MDIO1	I/O/PD	MII management data input/output transfers control information and status between the external PHY and the R2010C.

#### JTAG Enable Pin

PIN No.	Symbol	Type	Description
31	JTAGEN/SA3	I/O/PD	JTAG function enable. Default is pulled low and disabled. SA3: The slow bus address 3

#### SDRAM Interface

PIN No.	Symbol	Type	Description
73	SD_CLK	O	SDRAM clock output. This clock output is from internal De-skew PLL. It can be one to four multiple of input clock X1, depending on the setting of PFEREQ [0] during power-on resets.
63	MA11/A20	O	MA [11]: The SDRAM row and column address output Address bus 20. SDRAM module CKE must be tied high.
86	WE_n	O	SDRAM/EDO write enable.
85	CAS_n	O	SDRAM column address selector.
83	RAS_n	O	SDRAM row address selector.
81	BA0	O	SDRAM bank address 0.
80	BA1	O	SDRAM bank address 1.

87	DQML	O	Input/Output mask.
62	DQMH	O	Input/Output mask.

## Power Pins

PIN No.	Symbol	Type	Description
17,43,64,74, 92,101,124	VDDIO	I	I/O power pin, pure 3.3V.
1,35,53,72,82, 100,115	VSSIO	I	I/O ground pin.
22,57,99,122	VDDC	I	Core power pin, pure 2.5V.
6,40,84,104	VSSC	I	Core ground pin.
61	VDDP1	I	De-skew PLL power pin, pure 2.5V.
60	VSSP1	I	De-skew PLL ground pin.
3	VDDP2	I	Multiple PLL power pin, pure 2.5V.
2	VSSP2	I	Multiple PLL ground pin.

## Notes:

- When the PIO Mode register and PIO Direction register are configured as PIO modes, the 11 MUX definition pins can be used as PIO pins. For example, the PCS5\_n/PIO3 (Pin 125) can be used as a PIO3.
- In Normal Bus Mode (Bus Mode 1):  
I/O bus and Memory bus are all mapped to A [20:0] and D [15:0]. The SAD [15:0] bus is inactive in this mode.
- Change Bus Mode 0 and Bus Mode 1 by means of setting the internal Bus Control Register. This action must be initialized by software.
- Since all/partial Slow Bus Address, SA[11:0], on multiplexed pins are required, Bus Control Register should be enabled, then the default settings are disabled.

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## 3.3 PIN Capacitance Description

Symbol	Parameter	Min.	Typ.	Max.	Unit
C <sub>IN</sub>	3.3V Input Capacitance		2.8		pF
C <sub>OUT</sub>	3.3V Output Capacitance	2.7		4.9	pF
C <sub>BID</sub>	3.3V Bi-directional Capacitance	2.7		4.9	pF



### 3.4 PIN Pull-up/Pull-down Description

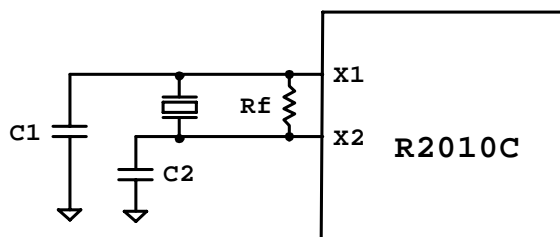
PIN Name	Pin No.	Pull-up	Pull-down	Schmitt Trigger	5V I/O Tolerant	Description (0.25uM)
RST_n ARDY	121 123	1	0	1	1	
INT0/SA11 INT1	7 5	0	1	0	1	
WR_n/BWSEL	39	1	0	0	1	
WLB_n/SA0	37	1	0	0	1	
TMROUT0/SA7 TMROUT1/SA8 /PIO	11 10	0	PIO10 PIO1	0	1	When set in normal operation, these two pins are with neither pull-up nor pull-down resistors. However, when set in PIO, they are input with pull-down resistors.
UCS_n MCS_n	98 97	1	0	1	0	
INT2 PCS0_n PCS2_n/IOR_n PCS3_n/IOW_n PCS5_n TMRIN0/SA9 TMRIN1/SA10 DRQ0/INT5/SA5 DRQ1/INT6/SA6 /PIO	4 126 33 34 125 9 8 13 12	PIO31 PIO14 PIO25 PIO26 PIO3 PIO11 PIO0 PIO12 PIO13	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	1	When set in normal operation, these pins are with neither pull-up nor pull-down resistors. However, when set in PIO, they are input with pull-up, pull-down, or schmitt trigger as listed in the left table.
DCD0_n SIN0 SOUT0 DTR0_n DSR0_n RI0_n RTS0_n CTS0_n /SAD15-8	21 14 15 18 20 23 16 19	1	0	0	1	
SOUT1 TCK TDI TMS	25 28 29 27	1	0	0	1	
SA4	30	1	0	0	1	
TXC1 RXC1	113 112	0	1	1	1	
RXD1_3 RXD1_2 RXD1_1 RXD1_0 RXDV1 COL1	111 110 109 108 107 120	0	1	0	1	

TXD1_3/PDIVID0 TXD1_0/PFREQ0	118 114	1	0	0	1	
TXD1_2/PDIVID1 TXD1_1/PDIVID2 TXEN1/CLKJMP	117 116 119	0	1	0	1	
MDIO1	105	0	1	0	1	
JTAGEN/SA3	31	0	1	1	1	
SA2	32				0	
CLKOUTA	103	0	0	0	0	
WHB_n/SA1	36	0	0	0	0	
RD_n	38	0	0	0	1	
A[17:19]/PIO	41,42,44	0	0	0	0	
A[0:10]	66~71 75~79	0	0	0	0	
A[11:16]	45~49 65	0	0	0	0	
D[0:15]	50~52 54~56 58~59 88~91 93~96	0	0	0	0	
SIN1	24	0	0	0	1	
RTS1_n/TDO	26	0	0	0	1	
MDC1	106	0	0	0	0	
SD_CLK	73	0	0	0	0	
WE_n CAS_n RAS_N BA[0:1] DQML DQMH	86 85 83 80~81 87 62	0	0	0	0	
A20/MA11	63	0	0	0	0	

**Note:** The pins never in the pull-up, pull-down, schmitt trigger, and I/O pad status are not shown in the above table.

## 4. Oscillator Characteristics

### 4.1 Fundamental Mode



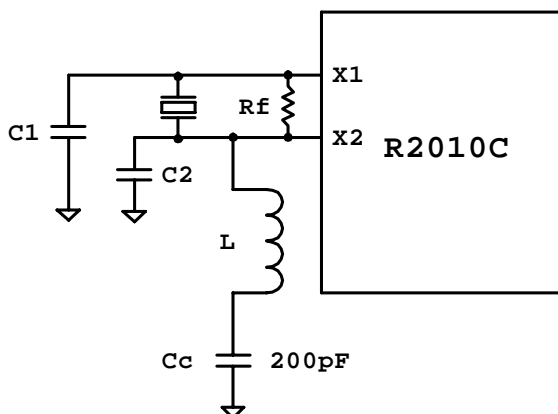
C1 ----- 20pF  $\pm$  20%

C2 ----- 20pF  $\pm$  20%

Rf ----- 1 mega-ohm

### 4.2 Third-Overtone Mode

Normally, high frequency use for third overtone mode can get price advantage, but additional L and Cc are needed.



Typical value suggestions are as follows:

C1 ----- 20pF  $\pm$  20%

C2 ----- 20pF  $\pm$  20%

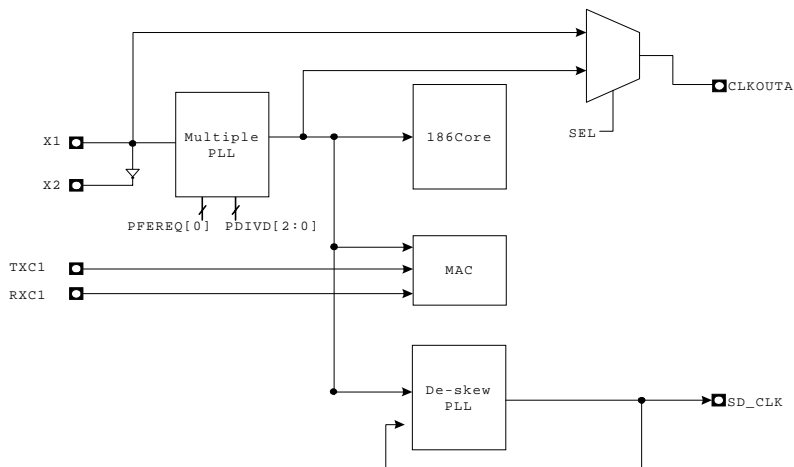
Cc ----- 200pF  $\pm$  20%

Rf ----- 1 Mega-Ohm

L ----- 4.7uH, 6.8uH, 8.2uH, 10uH (25MHz)

**Note:** X1 input clock must be within + - 100ppm tolerance.

## 5. Clock Unit



**PLL Configuration Table:**

Input Clock Range (Mhz)	PFEREQ[0]	PDIVD[2:0]			Multiple	Output Clock (Mhz)
25	1	0	0	0	1	25
		0	0	1	2	50
		0	1	0	3	75
		0	1	1	4	100
		1	0	0		Reserved
		1	0	1		Reserved
		1	1	0		Reserved
		1	1	1		Reserved
40	0	0	0	0	1	40
		0	0	1	2	80
		0	1	0		Reserved
		0	1	1		Reserved
		1	0	0		Reserved
		1	0	1		Reserved
		1	1	0		Reserved
		1	1	1		Reserved

For example: If input clock =25 Mhz, then set PFEREQ=1b.

If PDIVD[2:0]=000b, then PLL output clock =25 Mhz

If PDIVD[2:0]=011b, then PLL output clock =100 Mhz

## 6. Execution UNIT

### 6.1 General Registers

The R2010C has eight 16-bit general registers. And the AX, BX, CX, and DX can be subdivided into two 8-bit registers (AH, AL, BH, BL, CH, CL, DH and DL). The functions of these registers are described as follows:

**AX:** Word Divide, Word Multiply, Word I/O operation.

**AH:** Byte Divide, Byte Multiply, Byte I/O, Decimal Arithmetic, Translate operation.

**AL:** Byte Divide, Byte Multiply operation.

**BX:** Translate operation.

**CX:** Loops, String operation

**CL:** Variable Shift and Rotate operation.

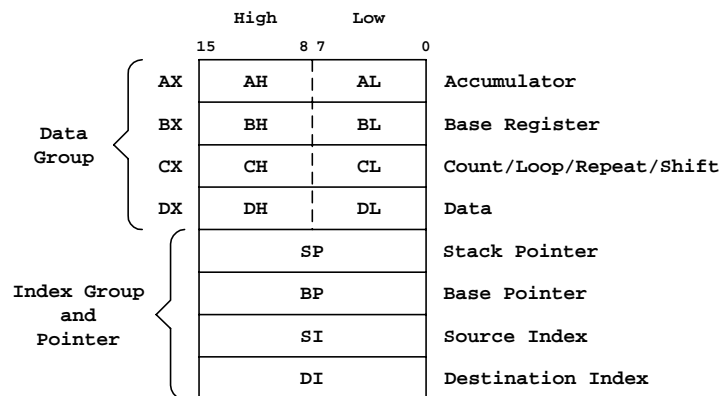
**DX:** Word Divide, Word Multiply, Indirect I/O operation

**SP:** Stack operations (POP, POPA, POPF, PUSH, PUSHA, PUSHF)

**BP:** General-purpose registers which can be used to determine offset address of operands in Memory.

**SI:** String operations

**DI:** String operations



**GENERAL REGISTERS**

### 6.2 Segment Registers

R2010C has four 16-bit segment registers: CS, DS, SS and ES. The segment registers contain the base addresses (starting location) of these memory segments, and they are immediately addressable for code (CS), data (DS & ES), and stack (SS) memory.

**CS (Code Segment):** The CS register points to the current code segment, which contains instruction to be fetched. The default location memory space for all instructions is 64K. The initial value of CS register is 0FFFFh.

**DS (Data Segment):** The DS register points to the current data segment, which generally contains program variables. The DS register is initialized to 0000H.

**SS (Stack Segment):** The SS register points to the current stack segment, which is for all stack operations, such as pushes and pops. The stack segment is used for temporary space. The SS register is initialized to 0000H.

**ES (Extra Segment):** The ES register points to the current extra segment, which is typically for data storage, such as large string operations and large data structures. The **ES** register is initialized to 0000H.

刪除: DS

15	8	7	0
CS			
Code Segment			
DS			
Data Segment			
SS			
Stack Segment			
ES			
Extra Segment			

#### SEGMENT REGISTERS

### 6.3 Instruction Pointer and Status Flags Registers

**IP (Instruction Pointer):** The IP is a 16-bit register and it contains the offset of the next instruction to be fetched. The IP register cannot be directly accessed by software. This register is update by the bus interface unit. It can be changed, saved or restored as a result of program execution. The IP register is initialized to 0000H and the starting execution address for CS:IP is at 0FFFF00H.

**Register Name:** Processor Status Flags Register

**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				OF	DF	IF	TF	SF	ZF	Rsvd	AF	Rsvd	PF	Rsvd	CF

These flags reflect the status after the Execution Unit is executed.

Bit	Name	Description
15-12	Rsvd	Reserved.
11	OF	Overflow Flag. If an arithmetic overflow occurs, this flag will be set.
10	DF	Direction Flag. If this flag is set, the string instructions are in the process of incrementing address. If DF is cleared, the string instructions are in the process of decrementing address. Refer to the STD and CLD instructions for how to set and clear the DF flag.
9	IF	Interrupt-Enable Flag. Refer to the STI and CLI instructions for how to set and clear the IF flag. Set to 1: The CPU enables the mask able interrupt request. Set to 0: The CPU disables the mask able interrupt request.
8	TF	Trace Flag. Set to enable single-step mode for debugging; Clear to disable the single-step mode. If an application program sets the TF flag with POPF or IRET instruction, a debug exception is generated after the instruction (The CPU automatically generates an interrupt after each instruction) that follows the POPF or IRET instruction.

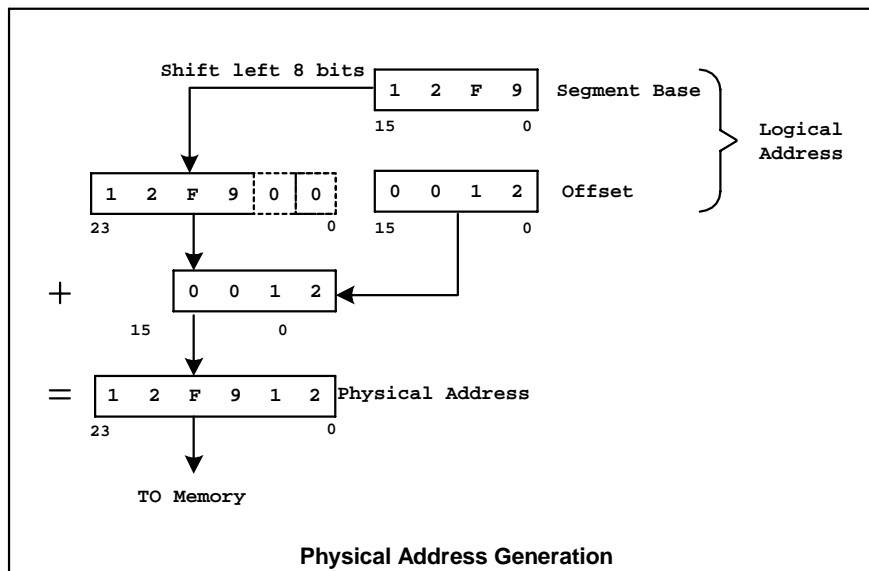
7	SF	Sign Flag. If this flag is set, the high-order bit of the result of an operation will be 1, indicating the state of being negative.
6	ZF	Zero Flag. If this flag is set, the result of operation will be zero.
5	Rsvd	Reserved
4	AF	Auxiliary Flag. If this flag is set, there will be a carry from the low nibble to the high one or a borrow from the high nibble to the low nibble of the AL general-purpose register. It is used in BCD operation.
3	Rsvd	Reserved
2	PF	This flag will be set if the result of the low-order 8 bits operation has even parity.
1	Rsvd	Reserved
0	CF	Carry Flag. If CF is set, there will be a carry out or a borrow into the high-order bit of the instruction result.

#### 6.4 Address Generation

The Execution Unit generates a 24-bit physical address to Bus Interface Unit by the Address Generation.

删除:

Memory is organized in sets of segments. Each segment contains a 16-bit value. Memory is addressed with a two-component address that consists of a 16-bit segment and 16-bit offset. The Physical Address Generation figure describes how the logical address is transferred to the physical address.



## 7. Peripheral Register List

The Peripheral Control Block can be mapped into either Memory or I/O space by programming the Peripheral Control Block Relocation Register (FEh). After reset, the default Legacy Peripheral Control Block offset is located at FF00h in I/O space, the SDRAM Control Register, EDO, Cache and Low speed clock is located at FE00h in I/O space, and Ethernet Control Register is located at FD00h and FE00h in I/O space.

The following table lists are all the definitions of the Peripheral Control Block Registers, and the detailed descriptions will be arranged on the related Block Unit.

### 7.1 Legacy Peripheral Registers (Base Address FF00h)

Offset (HEX)	Register Name	Page	Offset (HEX)	Register Name	Page
FE	Peripheral Control Block Relocation Register	28	74	PIO Data 0 Register	90
F8	Processor Extended ID Register	29	72	PIO Direction 0 Register	90
F6	Reset Configuration Register	31	70	PIO Mode 0 Register	90
F4	Processor Release Level Register	28	66	Timer 2 Mode / Control Register	69
F2	Auxiliary Configuration Register	35	62	Timer 2 Maxcount Compare A Register	70
EA	Bus Control Register	32	60	Timer 2 Count Register	70
E6	Watchdog Timer Control Register	71	5E	Timer 1 Mode / Control Register	67
E4	Enable RCU Register	43	5C	Timer 1 Maxcount Compare B Register	69
E2	Clock Prescaler Register	43	5A	Timer 1 Maxcount Compare A Register	68
DA	DMA 1 Control Register	59	58	Timer 1 Count Register	68
D8	DMA 1 Transfer Count Register	61	56	Timer 0 Mode / Control Register	65
D6	DMA 1 Destination Address High Register	61	54	Timer 0 Maxcount Compare B Register	66
D4	DMA 1 Destination Address Low Register	61	52	Timer 0 Maxcount Compare A Register	66
D2	DMA 1 Source Address High Register	62	50	Timer 0 Count Register	66
D0	DMA 1 Source Address Low Register	62	44	Serial Port 0 interrupt control register	46
CA	DMA 0 Control Register	57	42	Serial port 1 interrupt control register	46
C8	DMA 0 Transfer Count Register	57	40	MAC Interrupt Control Register	47
C6	DMA 0 Destination Address High Register	58	3C	INT2 Control Register	48
C4	DMA 0 Destination Address Low Register	58	3A	INT1 Control Register	48
C2	DMA 0 Source Address High Register	58	38	INT0 Control Register	49
C0	DMA 0 Source Address Low Register	59	36	DMA 1/INT6 Interrupt Control Register	50
AA	Chip Size Multiplier Register	41	34	DMA 0/INT5 Interrupt Control Register	50
AC	MCS_n Extended Register	42	32	Timer Interrupt Control Register	51
A8	PCS_n and MCS_n Auxiliary Register	40	30	Interrupt Status Register	51
A6	Midrange Chip Select Register	39	2E	Interrupt Request Register	52
A4	Peripheral Chip Select Register 0	38	2C	Interrupt In-service Register	52
A2	Low Memory Chip Select Register	37	2A	Interrupt Priority Mask Register	53
A0	Upper Memory Chip Select Register	36	28	Interrupt Mask Register	54
88	(See 7.2)	25	26	Interrupt Poll Status Register	54
86	(See 7.2)	25	24	Interrupt Poll Register	55



84	(See 7.2)	25	22	Interrupt End-of-Interrupt	55
82	(See 7.2)	25	18	(See 7.2)	25
80	(See 7.2)	25	16	(See 7.2)	25
7A	PIO Data 1 Register	89	14	(See 7.2)	25
78	PIO Direction 1 Register	89	12	(See 7.2)	25
76	PIO Mode 1 Register	89	10	(See 7.2)	25

## 7.2 16550 UART Register Definitions (Base Address FF00h)

Offset (HEX)	Register Name	Mnemonic	Page
80h	A Receiver Buffer Register (when DLAB=0 & Read)	RBR0	74
	UART0 Transmitter Holding Register (when DLAB=0 & Write)	THR0	75
	UART0 Divisor Latch [Low Byte] (when DLAB=1)	DLL0	75
82h	UART0 Interrupt Enable Register (when DLAB=0)	IER0	76
	UART0 Divisor Latch [High Byte] (when DLAB=1)	DLH0	75
84h	UART0 Interrupt Identification Register (when Read)	IIR0	77
	UART0 FIFO Control Register (when Write)	FCR0	78
86h	UART0 Line Control Register	LCR0	79
88h	UART0 MODEM Control Register	MCR0	80
8Ah	UART0 Line Status Register	LSR0	82
8Ch	UART0 MODEM Status Register	MSR0	84
8Eh	UART0 Scratch Register	SCR0	85
10h	UART1 Receiver Buffer Register (when DLAB=0 & Read)	RBR1	74
	UART1 Transmitter Holding Register (when DLAB=0 & Write)	THR1	75
	UART1 Divisor Latch [Low Byte] (when DLAB=1)	DLL1	75
12h	UART1 Interrupt Enable Register (when DLAB=0)	IER1	76
	UART1 Divisor Latch [High Byte] (when DLAB=1)	DLH1	75
14h	UART1 Interrupt Identification Register (when Read)	IIR1	77
	UART1 FIFO Control Register (when Write)	FCR1	78
16h	UART1 Line Control Register	LCR1	79
18h	UART1 MODEM Control Register	MCR1	80
1Ah	UART1 Line Status Register	LSR1	82
1Ch	UART1 MODEM Status Register	MSR1	84
1Eh	UART1 Scratch Register	SCR1	85

## 7.3 Cache control register (Base Address FEC0h)

Offset (HEX)	Register Name	Mnemonic	Page
C0h	Cache control register	CCR	91
C4h	Non-Cache region0 Starts Address High	NCR0SH	92
C2h	Non-Cache region0 Starts Address Low	NCR0SL	91
C8h	Non-Cache region0 End Address High	NCR0EH	92
C6h	Non-Cache region0 End Address Low	NCR0EL	92
CCh	Non-Cache region1 Starts Address High	NCR1SH	93
CAh	Non-Cache region1 Starts Address Low	NCR1SL	93
D0h	Non-Cache region1 End Address High	NCR1EH	94
CEh	Non-Cache region1 End Address Low	NCR1EL	93
D4h	Non-Cache region2 Starts Address High	NCR2SH	94

D2h	Non-Cache region2 Starts Address Low	NCR2SL	94
D8h	Non-Cache region2 End Address High	NCR2EH	95
D6h	Non-Cache region2 End Address Low	NCR2EL	95
DCh	Non-Cache region3 Starts Address High	NCR3SH	96
DAh	Non-Cache region3 Starts Address Low	NCR3SL	95
E0h	Non-Cache region3 End Address High	NCR3EH	96
DEh	Non-Cache region3 End Address Low	NCR3EL	96
E4h	Write-Invalidate region Starts Address High	WIRSH	97
E2h	Write-Invalidate region Starts Address Low	WIRSL	97
E8h	Write-Invalidate region End Address High	WIREH	98
E6h	Write-Invalidate region End Address Low	WIREL	97

#### 7.4 SDRAM Control Registers (Base Address FE00h)

格式化: 項目符號及編號

Offset (HEX)	Register Name	Mnemonic	Page
F2h	SDRAM Mode Set Register	SDRAMMSR	99
F4h	SDRAM Control Register	SDRAMCR	99
F6h	SDRAM Timing Parameter Register	SDRAMTPR	100

#### 7.5 Fast Ethernet MAC Control Registers (Base Address: MAC FE00h)

格式化: 項目符號及編號

Offset (HEX)	Register Name	Mnemonic	Page
00h	MAC Control Register 0	MCR0	106
04h	MAC Control Register 1	MCR1	107
08h	MAC Bus Control Register	MBCR	108
0Ch	TX Interrupt Control Register	MTICR	109
10h	RX Interrupt Control Register	MRICR	109
14h	TX Poll Command Register	MTPR	110
18h	RX Buffer Size Register	MRBSR	110
1Ah	RX Descriptor Control Register	MRDCR	111
1Ch	MAC Last Status Register	MLSR	111
20h	MAC MDIO Interface Register	MMDIO	112
24h	MAC MII Read Data Register	MMRD	113
28h	MAC MII Write Data Register	MMWD	113
2Ch	MAC TX Descriptor Start Address Register	MTDSA0	114
30h	MAC TX Descriptor Start Address Register	MTDSA1	114
34h	MAC RX Descriptor Start Address Register	MRDSA0	115
38h	MAC RX Descriptor Start Address Register	MRDSA1	115
3Ch	MAC INT Status Register	MISR	116
40h	MAC INT Enable Register	MIER	116
44h	MAC Event Counter INT Status Register	MECISR	117
48h	MAC Event Counter INT Mask Register	MECIER	118
50h	MAC Successfully Received Packet Counter	MRCNT	118
52h	MAC Event Counter 0 Register	MECNT0	119
54h	MAC Event Counter 1 Register	MECNT1	119
56h	MAC Event Counter 2 Register	MECNT2	120
58h	MAC Event Counter 3 Register	MECNT3	120
5Ah	MAC Successfully Transmit Packet Counter Register	MTCNT	121

刪除: 1

刪除: 2

5Ch	MAC Event Counter 4 Register	<b>MECNT4</b>	121
5Eh	MAC Pause Frame Counter Register	<b>MPCNT</b>	121
60h	MAC Hash Table Word 0	<b>MAR0</b>	122
62h	MAC Hash Table Word 1	<b>MAR1</b>	122
64h	MAC Hash Table Word 2	<b>MAR2</b>	123
66h	MAC Hash Table Word 3	<b>MAR3</b>	123
68h	MAC Multicast Address first two bytes Register	<b>MID0L</b>	124
6Ah	MAC Multicast Address second two bytes Register	<b>MID0M</b>	124
6Ch	MAC Multicast Address last two bytes Register	<b>MID0H</b>	124
70h	MAC Multicast Address first two bytes Register	<b>MID1L</b>	125
72h	MAC Multicast Address second two bytes Register	<b>MID1M</b>	125
74h	MAC Multicast Address last two bytes Register	<b>MID1H</b>	125
78h	MAC Multicast Address first two bytes Register	<b>MID2L</b>	126
7Ah	MAC Multicast Address second two bytes Register	<b>MID2M</b>	126
7Ch	MAC Multicast Address last two bytes Register	<b>MID2H</b>	126
80h	MAC Multicast Address first two bytes Register	<b>MID3L</b>	127
82h	MAC Multicast Address second two bytes Register	<b>MID3M</b>	127
84h	MAC Multicast Address last two bytes Register	<b>MID3H</b>	127

## 8. Peripheral Control Block Registers

The peripheral control block can be mapped into either memory or I/O space by programming the Peripheral Control Block Registers (FEh Registers). It starts at FF00h in I/O space after reset.

**Register Offset:** FEh  
**Register Name:** Peripheral Control Block Relocation Register  
**Reset Value :** 20FFh

删除: 0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			M/I/O_n	R[23:12] or R[19:8]											

The Peripheral Control Block (PCB) is mapped into either memory or I/O space by programming this register. When the other chip selects (PCsX\_n) are programmed to zero wait state and the external ready is ignored, PCsX\_n can overlap the control block.

Bit	Name	Attribute	Description
15-13	Rsvd	RO	Reserved.
12	M/I/O_n	R/W	Memory/I/O space. At reset, this bit is set to 0 and the PCB map starts at FF00h in I/O space. Set 1: The PCB is located in memory space. Set 0: The PCB is located in I/O space (Default).
11-0	R[23:12] or R[19:8]	R/W	Relocation Address Bits. The upper address bits of the PCB base address. In IO space, the lower eight bits are defaulted to 00h. When the PCB is mapped into I/O space, the R[19:16] must be programmed to 0000b. In memory space, R[19:8] are mapped into A[23:12] and the lower twelve bits are defaulted to 000h.

**Register Offset:** F4h  
**Register Name:** Processor Release Level Register  
**Reset Value :** 1AD9h

删除: 00

删除: 0

删除: 0

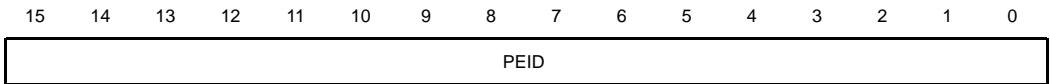
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	0	1	0	1	1	0	1	1	0	0	1

The read only registers specify the processor release version and RDC identification number.

Bit	Name	Attribute	Description
15-12	PRL	RO	4'b0001
11-8	PV	RO	Processor version.
7-0	ID	RO	RDC identification number 8'hD9.

**Register Offset:** F8h  
**Register Name:** Processor Extended ID Register  
**Reset Value :** 1602h

删除: 000



Bit	Name	Attribute	Description
15-0	PEID	RO	This read only register specifies the RDC identification extended number.

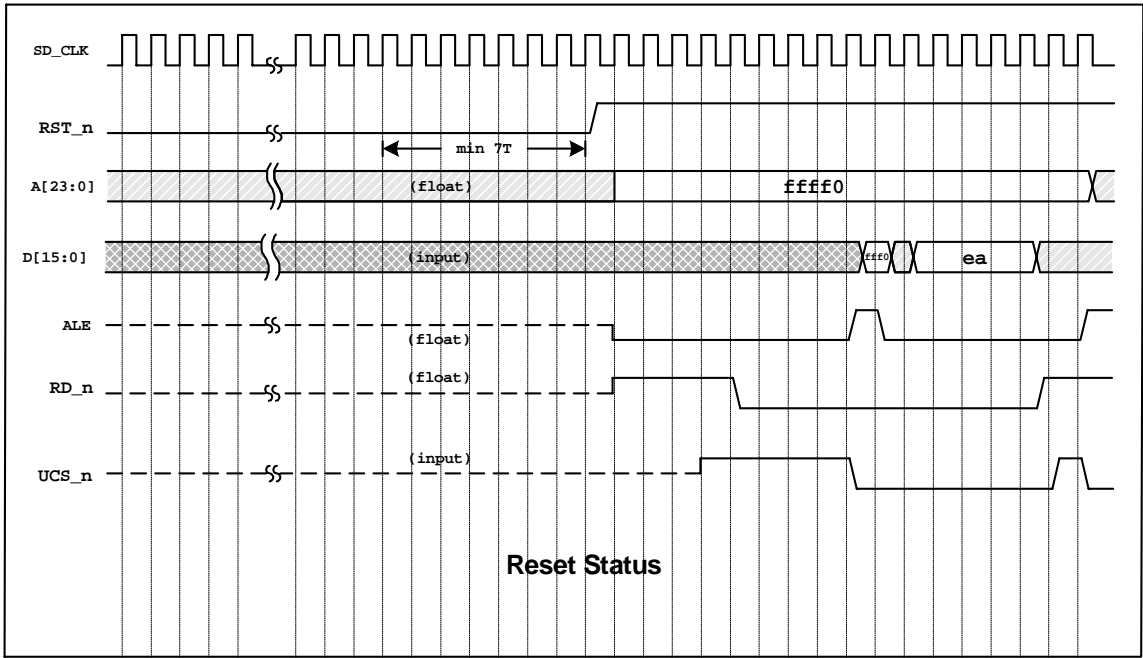
## 9. Reset

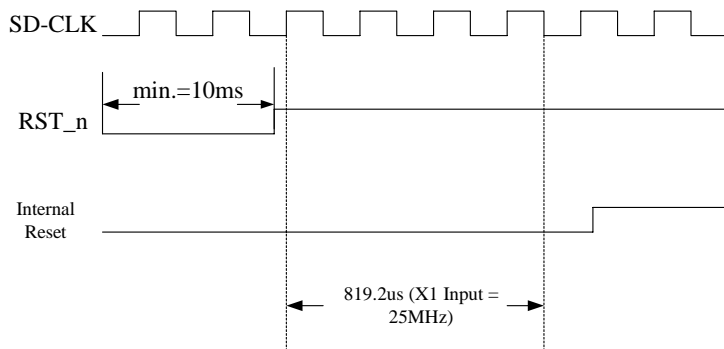
Processor initialization is accomplished with activation of the RST\_n pin. To reset the processor, this pin should be held low for at least seven oscillator periods. The Reset Status Figure shows the status of the RST\_n pin and the other related pins.

When RST\_n goes from low to high, the state of input pins (with weak pull-up or pull-down resistors) will be latched, and each pin will perform the individual function. The D[15:0] will be latched into the register F6h. UCS\_n/ONCE1\_n and LCS\_n/ONCE0\_n will enter ONCE mode (All of the pins will float except X1 and X2) when they are with pull-low resistors. The D[15:0] bus will not drive the address phase but the data phase during UCS\_n and LCS\_n cycles if WLB\_n is with a pull-high resistor.

刪除: low

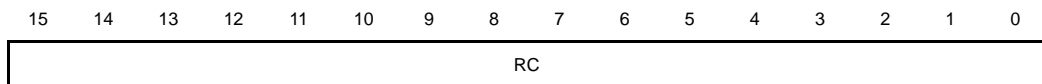
### 9.1 Power-up Reset





**Power-up Reset Timing**

**Register Offset:** F6h  
**Register Name:** Reset Configuration Register  
**Reset Value :** D[15:0]



Bit	Name	Attribute	Description
15-0	RC	RO	Reset Configuration D[15:0]. The D[15:0] must be with weak pull-up or pull-down resistors to correspond the contents when they are latched into this register as the RST_n signal goes from low to high. The value of the reset configuration register provides the system information when the software reads this register. This register is read only and the contents remain valid until next processor reset.

## 10. Bus Interface UNIT

### 10.1 Slow Bus

Register Offset: EAh  
Register Name: Bus Control Register  
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BMOD	Reserved							PCSE	SLAS			Reserved			

Bit	Name	Attribute	Description
15	BMOD	R/W	Bus Mode Select bit. <u>Set 0: Slow bus</u> mode. When the PCS/MCS regions are accessed, the bus cycle is mapped to SAD [15:0] or SAD [7:0]. Set 1: Normal <u>bus</u> mode. When the PCS/MCS regions are accessed, the bus cycle is mapped to A [23:0] and D [15:0]. The SAD bus is inactive in this mode.
14-7	Rsvd	R	Reserved
6	PCSE	R/W	IOR_n, IOW_n control signal enable When this bit is set. PIN36 is IOR_n and PIN37 is IOW_n. When this bit is clear. PIN36 is PCS2/PIO25 and PIN37 is PCS3/PIO26.
5-3	SLAS	R/W	SLA bus address selection bits 000: No slow bus address. 001: SLA5..0 010: SLA7..0 011: SLA11..0
2-0	Rsvd	R	Reserved

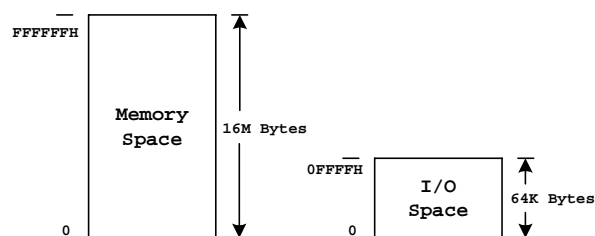
刪除: Shadow operation

刪除: operation

### 10.2 Memory and I/O Interface

The memory space consists of 16M bytes (8M 16-bit port) and the I/O space consists of 64k bytes (32k 16-bit port). Memory devices exchange information with the CPU during memory read, memory write and instruction fetch bus cycles. I/O read and I/O write bus cycles use a separate I/O address space. Only IN/OUT instruction can access I/O address space, and information must be transferred between the peripheral devices and the AX register. The first 256 bytes of I/O space can be accessed directly by the I/O instructions. The entire 64k bytes I/O address space can be accessed indirectly, through the DX register. I/O instructions always force address A[23:16] to low level.

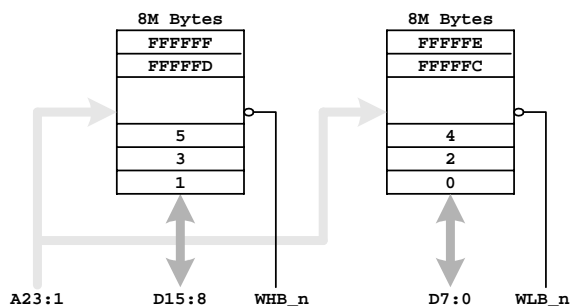




Memory and I/O Space

### 10.3 Data Bus

The memory address space data bus is physically implemented by dividing the address space into two banks of up to 8M bytes. Each bank connects to the lower half of the data bus and contains the even-addressed bytes (A0=0). The other bank connects to the upper half of the data bus and contains odd-addressed bytes (A0=1). WHB\_n and WLB\_n determine whether one bank or both banks participate in the data transfer.



Physical Data Bus Models

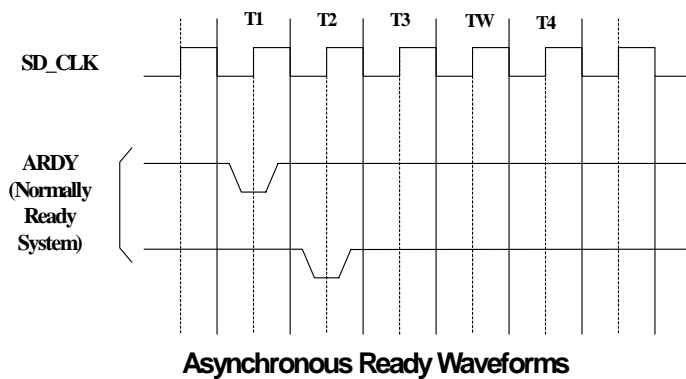
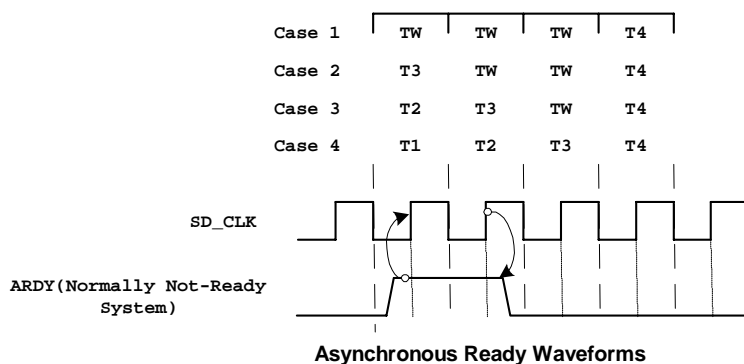
## 10.4 Wait States

Wait states extend the data phase of the bus cycle. The ARDY input with low level will insert wait states. To avoid wait states, ARDY must be high within a specified setup time prior to phase 2 of T1 and keep to phase 2 of T2. To insert wait states, ARDY must be driven low within a specified setup time prior to phase 2 of T1 or phase 2 of T2. When the SDRAMEN bit in the SDRAM Control Register (FEF4h) is set to 1, the external ready ARDY and internal wait states are ignored while accessing the SDRAMs.

删除: gh

删除: low

删除: high



## 10.5 Bus Width

The R2010C default is 16-bit bus access and the bus can be programmed as 8-bit or 16-bit access during memory or I/O access is located in the LCS\_n or PCSx\_n address space. The UCS\_n code- fetched selection can be 8-bit or 16-bit bus width, which is decided by the BWSEL pin (pin42) input status when the RST\_n pin goes from low to high. When the BWSEL pin is with a pull-low resistor, the bus width for the code-fetched selection is 8 bits. The SDRAM bus width is unchangeable 16 bits. If the R2010C has been set as 16-bit mode, it cannot be changed to 8-bit mode.

**Register Offset:** F2h  
**Register Name:** Auxiliary Configuration Register  
**Reset Value :** 0080h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	PCS5	PCS3	PCS2	0	Reserved		USIZ	0	0	0	0	0	0	MSIZ	PCS0

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14	PCS5	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.
13	PCS3	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.
12	PCS2	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.
11-8	Rsvd	RO	Reserved
7	USIZ	RO	Boot code bus width. This bit reflects the BWSEL pin input status when the RST_n pin goes from low to high. Set 0: 16-bit bus width booting when the BWSEL pin is <b>without a pull-low</b> resistor. (Default: It is an internal pull-high resistor.) Set 1: 8-bit bus width booting when the BWSEL pin is with a 4.7k ohm external pull-low resistor.
6-2	Rsvd	RO	Reserved
1	MSIZ	R/W	Midrange Data Bus Size selection. This bit determines the width of the data bus for all MCS and PCS space accesses (if mapped to memory space). 1: 8-bit data bus access. 0: 16-bit data bus access.
0	PCS0	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.

## 11. Chip Select UNIT

The Chip Select Unit provides 9 programmable chip select pins to access a specific memory or peripheral device. The chip selects are programmed through four peripheral control registers (A0h, A2h, A4h and A8h) and all the chip selects can insert wait states by programming the peripheral control registers.

### 11.1 UCS<sub>n</sub>

The UCS<sub>n</sub> default is active on reset for Code access. The active memory range is upper 8M (800000h – FFFFFFFh), which is programmable. And the default memory active range of UCS<sub>n</sub> is 64k (FF0000h – FFFFFFFh).

UCS<sub>n</sub> will drive low within four SD CLK cycles when active if no wait state is inserted. There are fifteen wait states inserted to UCS<sub>n</sub> active cycle on reset.

刪除: CLKOUTA

刪除: three

**Register Offset:** A0h  
**Register Name:** Upper Memory Chip Select Register  
**Reset Value :** F03Bh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	LB[2:0]		0	0	0	0	0	0	0	1	1	R3	R2	R1	R0

Bit	Name	Attribute	Description																																													
15	Rsvd	RO	Reserved.																																													
14-12	LB[2:0]	R/W	<b>LB[2:0]</b> , Memory block size selection for UCS_n chip select pin. The active region of the UCS_n chip select pin can be configured by LB[2:0]. The default memory block size is from 800000h to FFFFFFFh. Please refer to the following <b>Upper Memory Block Size</b> table for register FFAAh bit 5-3.																																													
11-4	Rsvd	RO	Reserved																																													
3	R3	R/W	See Bit[1:0].																																													
2	R2	R/W	Ready Mode. This bit is used to configure the ready mode for the UCS_n chip select. Set 1: external ready is ignored. Set 0: external ready is required.																																													
1-0	R[1:0]	R/W	<b>Bit3, Bit 1-0: R3, R[1:0]</b> , Wait-State value. R2010C can insert wait states for an access to the UCS_n memory cycle. The reset value for (R3, R1, R0) is (1, 1, 1). <table><tr><th>R3</th><th>R1</th><th>R0</th><th>--</th><th>Wait States</th></tr><tr><td>0</td><td>0</td><td>0</td><td>--</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>--</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>--</td><td>2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>--</td><td>3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>--</td><td>5</td></tr><tr><td>1</td><td>0</td><td>1</td><td>--</td><td>7</td></tr><tr><td>1</td><td>1</td><td>0</td><td>--</td><td>9</td></tr><tr><td>1</td><td>1</td><td>1</td><td>--</td><td>15</td></tr></table>	R3	R1	R0	--	Wait States	0	0	0	--	0	0	0	1	--	1	0	1	0	--	2	0	1	1	--	3	1	0	0	--	5	1	0	1	--	7	1	1	0	--	9	1	1	1	--	15
R3	R1	R0	--	Wait States																																												
0	0	0	--	0																																												
0	0	1	--	1																																												
0	1	0	--	2																																												
0	1	1	--	3																																												
1	0	0	--	5																																												
1	0	1	--	7																																												
1	1	0	--	9																																												
1	1	1	--	15																																												

刪除: When R2 is set to 0,

**Upper Memory Block Size table:**

FFAAh bit 5-3 \ LB[2:0]	000	100	110	111
000	512K	256K	128k	64k
001	1M	512K	256K	128k
010	2M	1M	512K	256K
011	X	2M	1M	512K
100	.X	X	2M	1M

## 11.2 LCS\_n

LCS\_n means the lower memory region chip selects. The active memory range is lower 8M (000000h – 7FFFFFFh), which is programmable. It can be expanded to 8M bytes by FFAAh b2:0.

**Register Offset:** A2h  
**Register Name:** Low Memory Chip Select Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		LB[2:0]	0	0	0	0	0	0	0	0	0	0	0	0	0

**删除:** 512k bytes  
(00000h-7FFFFFFh)

**删除:** So the A2h register must be programmed first before accessing the target memory range.

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14-12	LB[2:0]	R/W	<b>LB[2:0]</b> , Memory block size selection for the LCS_n chip select pin. The active region of the LCS_n chip select pin can be configured by LB[2:0].The LCS_n pin is not active on reset, but any read or write access to the Low Memory Chip Select Register (A2h) activates this pin. Please refer to the following <b>Low Memory Block Size</b> table for register FFAAh bit 2-0.
11-0	Rsvd	RO	Reserved

**Low Memory Block Size table:**

FFAAh bit2-0 \ LB[2:0]	000	001	011	111
000	64K	128K	256K	512K
001	128K	256K	512K	1M
010	256K	512K	1M	2M
011	512K	1M	2M	4M
100	1M	2M	4M	8M

### 11.3 PCS<sub>x</sub>\_n

In order to define these pins, the peripheral or memory chip selects are programmed through A4h and A8h registers. The base address memory block can be located anywhere within the 1M bytes memory space, exclusive of the areas associated with LCS<sub>n</sub> and UCS<sub>n</sub>. If the chip selects are mapped to I/O space, the access range is 64k bytes. PCS5<sub>n</sub> can be configured from (0 to 31 wait states) + (1 to 225 wait states). PCS3<sub>n</sub> – PCS0<sub>n</sub> can be configured from (1 to 31 wait states) + (1 to 225 wait states). The PCS<sub>x</sub>\_n pins are not active on reset. The PCS<sub>x</sub>\_n pins are activated as chip selects by writing to the peripheral chip select register 0 and 1.

**Register Offset:** A4h  
**Register Name:** Peripheral Chip Select Register 0  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA[19:12]								BA23	BA22	BA21	BA20	R3	R2	R1	R0

Bit	Name	Attribute	Description																																																																																																						
15-8	BA[19:12]	R/W	Base Address. BA[23:12] corresponds to Bit [23:12] of the 16M-Byte(24-bits) programmable base address of the PCS_n chip select block. When the PCS_n chip selects are mapped to I/O space, BA[23:16] must be written to 0000b because the I/O address bus is only 64K bytes (16-bits) wide. Please refer to the following <b>Peripheral Chip Size</b> table for register FFAAh bit 8-6.																																																																																																						
7-4	BA[23:20]	R/W																																																																																																							
3	R3	R/W	See Bit[1:0].																																																																																																						
2	R2	R/W	Ready Mode. This bit is configured to enable/disable the ready mode for the PCS3_n – PCS0_n chip selects. Set 1: external ready is ignored. Set 0: external ready is required.																																																																																																						
1-0	R[1:0]	R/W	<b>Bit 3, Bit 1-0: R3, R1, R0, Wait-State Values.</b> PR4 (refer to Bit 5 in the A8h register), R3, R1, and R0 determine the number of wait states inserted into T3 of the PCS3_n – PCS0_n access. <table><tr><th>PR4</th><th>R3</th><th>R1</th><th>R0</th><th>--</th><th><u>Wait States</u></th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>--</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>--</td><td>3</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>--</td><td>5</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>--</td><td>7</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>--</td><td>9</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>--</td><td>15</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>--</td><td>25</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>--</td><td>40</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>--</td><td>60</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>--</td><td>80</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>--</td><td>100</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>--</td><td>125</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>--</td><td>150</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>--</td><td>180</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>--</td><td>210</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>--</td><td>255</td></tr></table>	PR4	R3	R1	R0	--	<u>Wait States</u>	0	0	0	0	--	1	0	0	0	1	--	3	0	0	1	0	--	5	0	0	1	1	--	7	0	1	0	0	--	9	0	1	0	1	--	15	0	1	1	0	--	25	0	1	1	1	--	40	1	0	0	0	--	60	1	0	0	1	--	80	1	0	1	0	--	100	1	0	1	1	--	125	1	1	0	0	--	150	1	1	0	1	--	180	1	1	1	0	--	210	1	1	1	1	--	255
PR4	R3	R1	R0	--	<u>Wait States</u>																																																																																																				
0	0	0	0	--	1																																																																																																				
0	0	0	1	--	3																																																																																																				
0	0	1	0	--	5																																																																																																				
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1	0	0	1	--	80																																																																																																				
1	0	1	0	--	100																																																																																																				
1	0	1	1	--	125																																																																																																				
1	1	0	0	--	150																																																																																																				
1	1	0	1	--	180																																																																																																				
1	1	1	0	--	210																																																																																																				
1	1	1	1	--	255																																																																																																				

**Peripheral Chip Size table:**

FFAAh bit8-6	PCS0	PCS2	PCS3	PCS5
000	BASE	BASE+512	BASE+768	BASE+1280
001	BASE	BASE+1024	BASE+1536	BASE+2560
010	BASE	BASE+2048	BASE+3072	BASE+5120
011	BASE	BASE+4096	BASE+6144	BASE+10240
100	BASE	BASE+8192	BASE+12288	BASE+20480

## 11.4 MCS<sub>n</sub>

**Register Offset:** A6h  
**Register Name:** Midrange Chip Select Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA[19:12]								BA23	BA22	BA21	BA20	R3	R2	R1	R0

The base address can be set to any integer multiple of the size of the memory block size selected in this Midrange Chip Select Register. For example, if the midrange block is 16Kbytes, the block could be located at 100000h, 104000h, or 108000h, but not at 102000h.

Bit	Name	Attribute	Description																																																																														
15-4	BA[19:12]	R/W	Base Address. BA[23:12] corresponds to Bit [23:12] of the 16M-Byte (24-bits) programmable base address of the MCS chip select block.																																																																														
7-4	BA[23:20]	R/W																																																																															
3	R3	R/W	See Bit[1:0].																																																																														
2	R2	R/W	Ready Mode. This bit is configured to enable/disable the ready mode for the MCS chip selects. Set 1: external ready is ignored. Set 0: external ready is required.																																																																														
1-0	R[1:0]	R/W	<b>Bit 3, Bit 1-0: R3, R1, R0, Wait-State Values.</b> R3, R1, and R0 determine the number of wait states inserted into T3 of the MCS3_n – MCS0_n access. With regard to the values of R4, please refer to bit 4 in the FFACH register. <table><tr><th>R4,</th><th>R3,</th><th>R1,</th><th>R0</th><th>--</th><th><u>Wait States</u></th></tr><tr><td>0,</td><td>0,</td><td>0,</td><td>0</td><td>--</td><td>1</td></tr><tr><td>0,</td><td>0,</td><td>0,</td><td>1</td><td>--</td><td>3</td></tr><tr><td>0,</td><td>0,</td><td>1,</td><td>0</td><td>--</td><td>5</td></tr><tr><td>0,</td><td>0,</td><td>1,</td><td>1</td><td>--</td><td>7</td></tr><tr><td>0,</td><td>1,</td><td>0,</td><td>0</td><td>--</td><td>9</td></tr><tr><td>0,</td><td>1,</td><td>0,</td><td>1</td><td>--</td><td>15</td></tr><tr><td>0,</td><td>1,</td><td>1,</td><td>0</td><td>--</td><td>25</td></tr><tr><td>0,</td><td>1,</td><td>1,</td><td>1</td><td>--</td><td>40</td></tr><tr><td>1,</td><td>0,</td><td>0,</td><td>0</td><td>--</td><td>60</td></tr><tr><td>1,</td><td>0,</td><td>0,</td><td>1</td><td>--</td><td>80</td></tr><tr><td>1,</td><td>0,</td><td>1,</td><td>0</td><td>--</td><td>100</td></tr><tr><td>1,</td><td>0,</td><td>1,</td><td>1</td><td>--</td><td>125</td></tr></table>	R4,	R3,	R1,	R0	--	<u>Wait States</u>	0,	0,	0,	0	--	1	0,	0,	0,	1	--	3	0,	0,	1,	0	--	5	0,	0,	1,	1	--	7	0,	1,	0,	0	--	9	0,	1,	0,	1	--	15	0,	1,	1,	0	--	25	0,	1,	1,	1	--	40	1,	0,	0,	0	--	60	1,	0,	0,	1	--	80	1,	0,	1,	0	--	100	1,	0,	1,	1	--	125
R4,	R3,	R1,	R0	--	<u>Wait States</u>																																																																												
0,	0,	0,	0	--	1																																																																												
0,	0,	0,	1	--	3																																																																												
0,	0,	1,	0	--	5																																																																												
0,	0,	1,	1	--	7																																																																												
0,	1,	0,	0	--	9																																																																												
0,	1,	0,	1	--	15																																																																												
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0,	1,	1,	1	--	40																																																																												
1,	0,	0,	0	--	60																																																																												
1,	0,	0,	1	--	80																																																																												
1,	0,	1,	0	--	100																																																																												
1,	0,	1,	1	--	125																																																																												

			1, 1, 0, 0 -- 150
			1, 1, 0, 1 -- 180
			1, 1, 1, 0 -- 210
			1, 1, 1, 1 -- 255

**Register Offset:** A8h  
**Register Name:** PCS\_n and MCS\_n Auxiliary Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	M[6:0]							Rsvd	MS	PR4	R4	R3	R2	R1	R0

Bit	Name	Attribute	Description																																																																																										
15	Rsvd	RO	Reserved																																																																																										
14-8	M[6:0]	R/W	MCS_n Block Size (M[6:0]). Please refer to the following <b>Midrange Memory Block Size</b> table for register FFAAh bit 11-9.																																																																																										
7	Rsvd	RO	Reserved																																																																																										
6	MS	R/W	Memory or IO space selector. This bit determines whether the PCS_n pins are active during memory bus cycle or IO bus cycle. Set 1: PCS_n active for memory cycle. Set 0: PCS_n active for IO cycle.																																																																																										
5-4	PR4	R/W	See bit[1:0] in the A4h register.																																																																																										
4-3	R[4:3]	R/W	See bit[1:0]																																																																																										
2	R2	R/W	Ready Mode. This bit only applies to the PCS5_n chip select. Set 1: external ready is ignored. Set 0: external ready is required.																																																																																										
1-0	R[1:0]	R/W	<b>Bit 4-3 and Bit 1-0: R4, R3, R1, R0, Wait-State Values.</b> R4, R3, R1, and R0 determine the number of wait states inserted into T3 of the PCS5_n access. <table><tr><th>R4</th><th>R3</th><th>R1</th><th>R0</th><th>--</th><th><u>Wait States</u></th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>--</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>--</td><td>3</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>--</td><td>5</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>--</td><td>7</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>--</td><td>9</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>--</td><td>15</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>--</td><td>25</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>--</td><td>40</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>--</td><td>60</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>--</td><td>80</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>--</td><td>100</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>--</td><td>125</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>--</td><td>150</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>--</td><td>180</td></tr></table>	R4	R3	R1	R0	--	<u>Wait States</u>	0	0	0	0	--	1	0	0	0	1	--	3	0	0	1	0	--	5	0	0	1	1	--	7	0	1	0	0	--	9	0	1	0	1	--	15	0	1	1	0	--	25	0	1	1	1	--	40	1	0	0	0	--	60	1	0	0	1	--	80	1	0	1	0	--	100	1	0	1	1	--	125	1	1	0	0	--	150	1	1	0	1	--	180
R4	R3	R1	R0	--	<u>Wait States</u>																																																																																								
0	0	0	0	--	1																																																																																								
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0	1	0	1	--	15																																																																																								
0	1	1	0	--	25																																																																																								
0	1	1	1	--	40																																																																																								
1	0	0	0	--	60																																																																																								
1	0	0	1	--	80																																																																																								
1	0	1	0	--	100																																																																																								
1	0	1	1	--	125																																																																																								
1	1	0	0	--	150																																																																																								
1	1	0	1	--	180																																																																																								



			1, 1, 1, 0 -- 210
			1, 1, 1, 1 -- 255

**Midrange Memory Block Size table:**

FFAAh bit11-9					
Total Block Size 000	Total Block Size 001	Total Block Size 010	Total Block Size 011	Total Block Size 100	M[6:0]
8K	16K	32K	64K	128K	0000001b
16K	32K	64K	128K	256K	0000010b
32K	64K	128K	256K	512K	0000100b
64K	128K	256K	512K	1M	0001000b
128K	256K	512K	1M	2M	0010000b
256K	512K	1K	2M	X	0100000b
512K	1M	2M	X	X	1000000b

**Register Offset:** AAh  
**Register Name:** Chip Size Multiplier Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	W[2:0]		M[2:0]		P[2:0]		U[2:0]		L[2:0]						

Bit	Name	Attribute	Description
15	Rsvd	R	Reserved
14-12	W[2:0]	R/W	Wait-State Value. W[2:0] determine the number of wait states inserted into T1 of PCS5_n and the PCS3_n – PCS0_n access. <div style="display: flex; justify-content: space-between;"> <div>W2, W1, W0 --</div> <div><u>Wait States</u></div> </div> <div style="display: flex; justify-content: space-between;"> <div>0, 0, 0 --</div> <div>0</div> </div> <div style="display: flex; justify-content: space-between;"> <div>0, 0, 1 --</div> <div>1</div> </div> <div style="display: flex; justify-content: space-between;"> <div>0, 1, 0 --</div> <div>3</div> </div> <div style="display: flex; justify-content: space-between;"> <div>0, 1, 1 --</div> <div>7</div> </div> <div style="display: flex; justify-content: space-between;"> <div>1, 0, 0 --</div> <div>11</div> </div> <div style="display: flex; justify-content: space-between;"> <div>1, 0, 1 --</div> <div>15</div> </div> <div style="display: flex; justify-content: space-between;"> <div>1, 1, 0 --</div> <div>20</div> </div> <div style="display: flex; justify-content: space-between;"> <div>1, 1, 1 --</div> <div>31</div> </div>
11-9	M[2:0]	R/W	MCS chip select size multiplier
8-6	P[2:0]	R/W	PCS chip select size multiplier
5-3	U[2:0]	R/W	UCS chip select size multiplier
2-0	L[2:0]	R/W	LCS chip select size multiplier

**Register Offset:** ACh  
**Register Name:** MCS\_n Extended Register  
**Reset Value :** 00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	R4	0	W2	W1	W0

Bit	Name	Attribute	Description
15-5	Rsvd	R/O	Defaulted as 0.
4	R4	R/W	Defaulted as 0. Please see the description for bit 1-0 in the A6h register.
3	Rsvd	RO	Defaulted as 0
2-0	W[2:0]	R/W	T1 Wait-State Value. Defaulted as 0.

## 12. Refresh Control UNIT

The Refresh Control Unit (RCU) automatically generates refresh bus cycle. After a period of time, the RCU generates a memory read request to the bus interface unit.

A user guide to program SDRAM:

(1) Configure Lower Memory Chip Select Register (A2h) to set SDRAM space. The suggestion value is 7F38h.

(2) Set Clock Prescaler Register (E2h) and RCU Register (E4h) to enable SDRAM refresh.

**删除:** The Refresh Control Unit operates when the internal clock is off. If the power-save mode is in effect, the Refresh Control Unit must be reprogrammed to reflect the new clock rate.

**Register Offset:** E2h

**Register Name:** Clock Prescaler Register

**Reset Value :** 0080h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RC[14:0]														

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14-0	RC[14:0]	RW	Refresh Counter Reload Value. It contains the value of the desired clock count interval between refresh cycles. The counter value should not be set to less than 12h, otherwise there would never be sufficient bus cycle available for the processor to execute code. For Example: SDRAM specification specifies to refresh 1 time every 15.6 u sec and system clock is 25Mhz. The Refresh Counter Reload Value = $15.6\mu s * 25\text{Mhz} = 15.6\mu s / 40\text{ns} = 390$ .

**Register Offset:** E4h

**Register Name:** Enable RCU Register

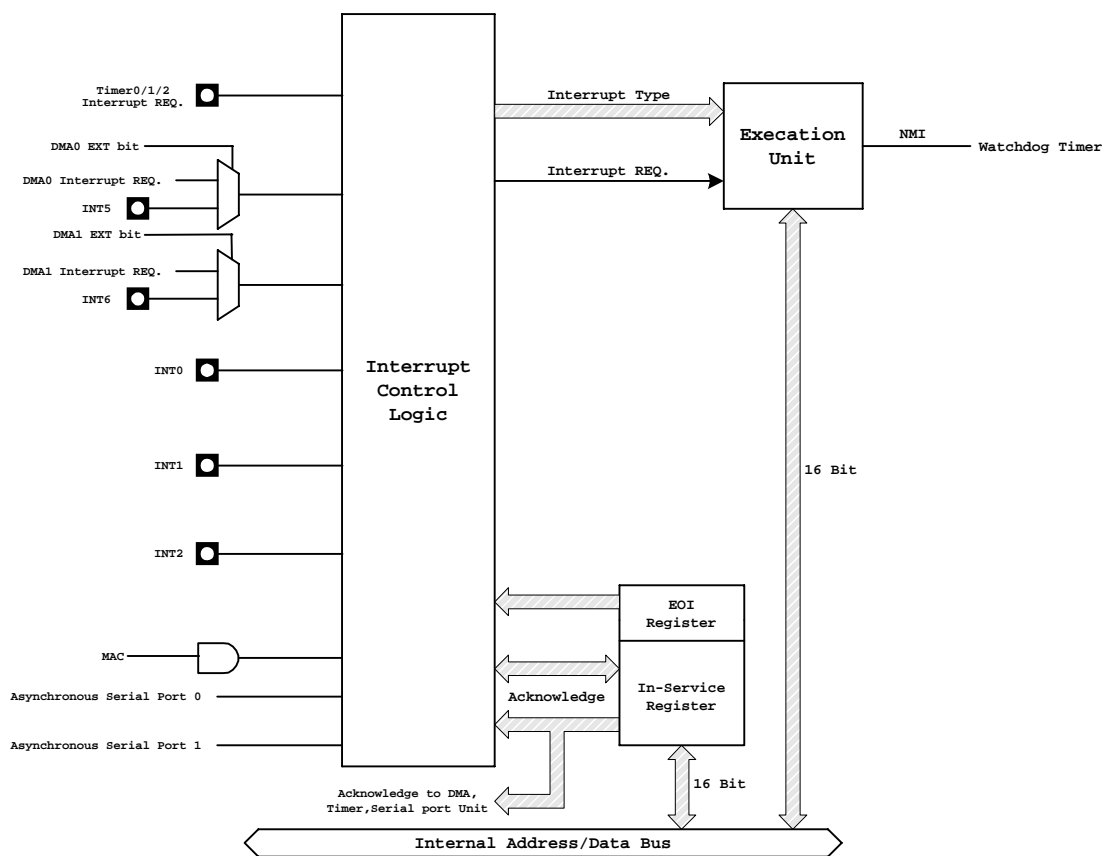
**Reset Value :** 8000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E	T[14:0]														

Bit	Name	Attribute	Description
15	E	RW	Enable RCU Set 1: Enable the refresh counter unit. Set 0: Clear the refresh counter and stop refresh requests, but will not reset the refresh address.
14-0	T[14:0]	RO	Refresh Count. This read-only field contains the present value of the down counter which triggers refresh requests.

### 13. Interrupt Controller UNIT

There are 14 interrupt request sources connected to the controller: 5 maskable interrupt pins (INT[0:2], INT5, INT6); 1 non-mask able interrupts (WDT); 8 internal unit request sources (Timer 0, 1, 2; DMA 0, 1; MAC; Asynchronous Serial Port 0, 1).



Interrupt Control Unit Block Diagram

### 13.1 Interrupt Vector, Type and Priority

The following table shows the interrupt vector address, type and the priority. The maskable interrupt priority can be changed by programming the priority registers. The vector address for each interrupt was fixed.

Interrupt source	Interrupt Type	Vector Address	EOI Type	Priority	Note
Divide Error Exception	00h	00h		1	
Trace interrupt	01h	04h		1-1	*
NMI	02h	08h		1-2	*
Breakpoint Interrupt	03h	0Ch		1	
INT0 Detected Over Flow Exception	04h	10h		1	
Array Bounds Exception	05h	14h		1	
Undefined Op code Exception	06h	18h		1	
ESC Op code Exception	07h	1Ch		1	
Timer 0	08h	20h	08	2-1	*
Reserved	09h				
DMA 0/INT5	0Ah	28h	0A	3	
DMA 1/INT6	0Bh	2Ch	0B	4	
INT0	0Ch	30h	0C	5	
INT1	0Dh	34h	0D	6	
INT2	0Eh	38h	0E	7	
MAC	10h	40h	10	9	
Asynchronous Serial port 1	11h	44h	11	9	
Timer 1	12h	48h	08	2-2	*
Timer 2	13h	4Ch	08	2-3	*
Asynchronous Serial port 0	14h	50h	14	9	
Reserved	15h-1Fh				

Note \*: When the interrupt occurs in the same time, the priority is (1-1 > 1-2); (2-1 > 2-2 > 2-3)

### 13.2 Interrupt Requests

When an interrupt is requested, the internal interrupt controller verifies the interrupt is enabled (the IF flag is enabled and the MSK bit is not set) and that there are no higher priority interrupt requests being serviced or pending. If the interrupt is granted, the interrupt controller uses the interrupt type to access a vector from the interrupt vector table.

If the external INT is active (level-trigger) to request the interrupt controller service, the INT pins must be held till the micro controller entering the interrupt service routine. There is no interrupt-acknowledge output when running in fully nested mode, so it should use PIO pin to simulate the interrupt-acknowledge pin if necessary.

### 13.3 Programming the Registers

Software is programmed through the registers (44h, 42h, 40h, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h, 26h, 24h and 22h) to define the interrupt controller operation.

**Register Offset:** 44h  
**Register Name:** Serial Port 0 Interrupt Control Register  
**Reset Value :** 001Fh

删除: 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											1	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the asynchronous serial port 0. Set 0: Enable the serial port 0 interrupt.
2-0	PR[2:0]	R/W	Priority. These bits determine the priorities of the serial ports relative to the other interrupt signals. <b>The priority selection:</b> <b>PR2, PR1, PR0 -- Priority</b> 0 , 0 , 0 -- 0 (High) 0 , 0 , 1 -- 1 0 , 1 , 0 -- 2 0 , 1 , 1 -- 3 1 , 0 , 0 -- 4 1 , 0 , 1 -- 5 1 , 1 , 0 -- 6 1 , 1 , 1 -- 7 (Low)

**Register Offset:** 42h  
**Register Name:** Serial Port 1 Interrupt Control Register  
**Reset Value :** 001Fh

删除: 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											1	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the asynchronous serial port 1. Set 0: Enable the serial port 1 interrupt.
2-0	PR[2:0]	R/W	Priority. These bits determine the priorities of the serial ports relative to the other interrupt signals.  <b>The priority selection:</b> <b>PR2, PR1, PR0 -- Priority</b> 0 , 0 , 0 -- 0 (High) 0 , 0 , 1 -- 1 0 , 1 , 0 -- 2 0 , 1 , 1 -- 3 1 , 0 , 0 -- 4 1 , 0 , 1 -- 5 1 , 1 , 0 -- 6 1 , 1 , 1 -- 7 (Low)

**Register Offset:** 40h  
**Register Name:** MAC Interrupt Control Register  
**Reset Value :** 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Reserved	LTM	MSK	PR2	PR1	PR0	

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enable. When this bit is set to 1 and bit 4 is <u>cleared</u> to 0, an interrupt is triggered by edge from MAC, which goes from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6-5	Rsvd	RO	Reserved
4	LTM	R/W	Level-Triggered Mode. Set 1: the high active level triggers an interrupt. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of MAC. Set 0: Enable the MAC interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

删除: set

**Register Offset:** 3Ch  
**Register Name:** INT2 Control Register  
**Reset Value :** 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Rsvd	ES	LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enable. When this bit is set and bit 4 is <u>cleared</u> to 0, an interrupt is triggered by the edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6	Rsvd	RO	Reserved
5	ES	R/W	Edge Select Set 1 = Falling edge/Low level trigger. Set 0 = Rising edge/High level trigger.
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by the high active level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT2. Set 0: Enable the INT2 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

刪除: set

**Register Offset:** 3Ah  
**Register Name:** INT1 Control Register  
**Reset Value :** 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	ES	LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enable. When this bit is set and bit 4 is <u>cleared</u> to 0, an interrupt is triggered by the edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6	SFNM	R/W	Special Fully Nested Mode. Set 1: Enable the special fully nested mode of INT1
5	ES	R/W	Edge Select

刪除: set



			Set 1: falling edge / Low level trigger Set 0: rising edge /High level trigger
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by the high active level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT1. Set 0: Enable the INT1 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

**Register Offset:** 38h  
**Register Name:** INT0 Control Register  
**Reset Value :** 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	ES	LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enable. When this bit is set and bit 4 is <u>cleared</u> to 0, an interrupt is triggered by the edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6	SFNM	R/W	Special Fully Nested Mode. Set 1: Enable the special fully nested mode of INT0
5	ES	R/W	Edge Select Set 1: Falling edge/Low level trigger. Set 0 : Rising edge/High level trigger.
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by the high active level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT0. Set 0: Enable the INT0 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

删除: set

**Register Offset:** 36h  
**Register Name:** DMA1/INT6 Interrupt Control Register  
**Reset Value :** 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	ES	0	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved
5	ES	R/W	Edge Select Set 1: Falling edge/Low level trigger. Set 0: Rising edge/High level trigger.
4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the DMA1 controller. Set 0: Enable the DMA1 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

**Register Offset:** 34h  
**Register Name:** DMA0/INT5 Interrupt Control Register  
**Reset Value :** 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	ES	0	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved
5	ES	R/W	Edge Select Set 1 = Falling edge/Low level trigger. Set 0 = Rising edge/High level trigger.
4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the DMA0 controller. Set 0: Enable the DMA0 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

**Register Offset:** 32h  
**Register Name:** Timer Interrupt Control Register  
**Reset Value :** 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the timer controller. Set 0: Enable the timer controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

**Register Offset:** 30h  
**Register Name:** Interrupt Status Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DHLT	Reserved								MAC	Rsvd	TMR2	TMR1	TMR0		

The **reset value** is not defined.

Bit	Name	Attribute	Description
15	DHLT	RO	DMA Halt. Set 1: Halt any DMA activity when non-mask able interrupts occur. Set 0: When an IRET instruction is executed.
14-6	Rsvd	RO	Reserved
5	MAC	RO	Indicate that the MAC controller has an interrupt request while set to 1.
4-3	Rsvd	RO	Reserved
2-0	TMR[2:0]	R/W	Indicate that the corresponding timer has an interrupt request pending while set to 1.

删除: pending

**Register Offset:** 2Eh  
**Register Name:** Interrupt Request Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				SP0	SP1	MAC	I3	I2	I1	I0	D1/I6	D0/I5	Rsvd	TMR	

The Interrupt Request register is a read-only register. For internal interrupts (SP0, SP1, D1/I6, D0/I5, MAC, and TMR), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge. For INT[2:0] external interrupts, the corresponding bits (I[3:0]) reflect the current values of the external signals.

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
10	SP0	RO	Serial Port 0 Interrupt Request. Indicates the interrupt status of the serial port 0.
9	SP1	RO	Serial Port 1 Interrupt Request. Indicates the interrupt status of the serial port 1.
8	MAC	RO	MAC Interrupt Request. Indicates the interrupt status of the MAC.
7-4	I[3:0]	RO	Interrupt Requests. Set 1: The corresponding INT pin has an interrupt pending.
3-2	D1/I6 – D0/I5	RO	DMA Channel or INT Interrupt Request. Set 1: The corresponding DMA channel or INT has an interrupt pending.
1	Rsvd	RO	Reserved
0	TMR	RO	Timer Interrupt Request. Set 1: The timer control unit has an interrupt pending.

删除: 1

删除: 1

删除: 1

删除: 1

删除: 1

删除: 1

删除: 1

删除: 1

删除: R/W

删除: 1

删除: R/W

删除: 1

删除: R/W

**Register Offset:** 2Ch  
**Register Name:** In-Service Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				SP0	SP1	MAC	I3	I2	I1	I0	D1/I6	D0/I5	Rsvd	TMR	

These bits in this Register are set by the interrupt controller when the interrupt is taken. Each bit in the register is cleared by writing the corresponding interrupt type to the EOI register.

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
10	SP0	R/W	Serial Port 0 Interrupt In-Service. Set 1: the serial port 0 interrupt is currently being serviced.

删除: 1

删除: 1

删除: 1

删除: 1

删除: 1

删除: 1

9	SP1	R/W	Serial Port 1 Interrupt In-Service. Set 1: the serial port 1 interrupt is currently being serviced.
8	MAC	R/W	MAC In-Service. Indicates the MAC interrupt is currently being serviced.
7-4	<del>↓[3:0]</del>	R/W	Interrupt In-Service. <del>Set 1: the corresponding INT interrupt is currently being serviced.</del>
3-2	<del>D1/6 – D0/5</del>	R/W	DMA Channel or INT Interrupt In-Service. <del>Set 1: the corresponding DMA channel or INT interrupt is currently being serviced.</del>
1	Rsvd	RO	Reserved
0	TMR	R/W	Timer Interrupt In-Service. Set 1: the timer interrupt is currently being serviced.

删除: 1

删除: 1

删除: 1

删除: 1

**Register Offset:** 2Ah  
**Register Name:** Priority Mask Register  
**Reset Value :** 0007h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	PRM2	PRM1	PRM0

It determines the minimum priority level at which mask able interrupts can generate interrupts.

Bit	Name	Attribute	Description																		
15-3	Rsvd	RO	Reserved																		
2-0	PRM[2:0]	R/W	<div>Priority Field Mask, determining the minimum priority that is required in order for a mask able interrupt source to generate an interrupt.</div> <table><thead><tr><th><u>PR[2:0]</u></th><th><u>Priority</u></th></tr></thead><tbody><tr><td>000</td><td>(High) 0</td></tr><tr><td>001</td><td>1</td></tr><tr><td>010</td><td>2</td></tr><tr><td>011</td><td>3</td></tr><tr><td>100</td><td>4</td></tr><tr><td>101</td><td>5</td></tr><tr><td>110</td><td>6</td></tr><tr><td>111</td><td>(Low) 7</td></tr></tbody></table>	<u>PR[2:0]</u>	<u>Priority</u>	000	(High) 0	001	1	010	2	011	3	100	4	101	5	110	6	111	(Low) 7
<u>PR[2:0]</u>	<u>Priority</u>																				
000	(High) 0																				
001	1																				
010	2																				
011	3																				
100	4																				
101	5																				
110	6																				
111	(Low) 7																				

**Register Offset:** 28h  
**Register Name:** Interrupt Mask Register  
**Reset Value :** FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				SP0	SP1	MAC	↓3	↓2	↓1	↓0	D1↓6	D0↓5	Rsvd	TMR	

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
10	SP0	R/W	Serial Port 0 Interrupt Mask. When set 1, this bit indicates that the asynchronous serial port 0 interrupt is masked.
9	SP1	R/W	Serial Port 1 Interrupt Mask. When set 1, this bit indicates that the asynchronous serial port 1 interrupt is masked.
8	MAC	R/W	MAC Interrupt Mask. When set 1, this bit indicates that the MAC interrupt is masked.
7-4	↓[3:0]	R/W	External Interrupt Mask. When set 1, I3-I0 bits indicate that the corresponding interrupts are masked.
3-2	D1↓6 – D0↓5	R/W	DMA Channel or INT Interrupt Masks. When set 1, these bits indicate that the corresponding interrupts are masked.
1	Rsvd	RO	Reserved
0	TMR	R/W	Timer Interrupt Mask. When set 1, this bit indicates that the Timer controller interrupt is masked.

删除: 0

删除: 1

删除: 1

删除: 1

删除: 1

删除: 1

删除: 1

删除: 1

删除: 1

删除: 1

删除: 1

**Register Offset:** 26h  
**Register Name:** Poll Status Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IREQ	Reserved										S[4:0]				

The Poll Status (POLLST) register mirrors the current state of the Poll register. The POLLST register can be read without affecting the current interrupt requests.

Bit	Name	Attribute	Description
15	IREQ	R/W	Interrupt Request. Set 1: if an interrupt is pending. The S[4:0] field contains valid data.
14-5	Rsvd	RO	Reserved
4-0	S[4:0]	R/W	Poll Status. It indicates the interrupt type of the highest priority pending interrupts.

**Register Offset:** 24h  
**Register Name:** Poll Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IREQ	Reserved										S[4:0]				

When the Poll register is read, the current interrupt is acknowledged and the next interrupt takes its place in the Poll register.

Bit	Name	Attribute	Description
15	IREQ	R/W	Interrupt Request. Set 1: if an interrupt is pending. The S[4:0] field contains valid data.
14-5	Rsvd	RO	Reserved
4-0	S[4:0]	R/W	Poll Status. It indicates the interrupt type of the highest priority pending interrupts.

**Register Offset:** 22h  
**Register Name:** End - Of - Interrupt  
**Reset Value :** Write Only

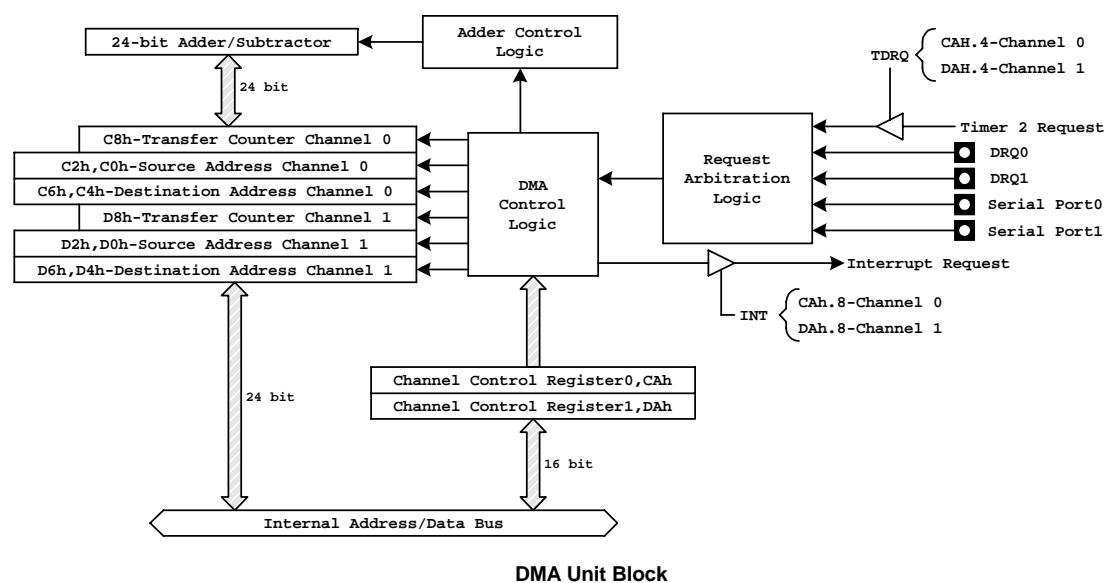
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NSPEC	Reserved										S[4:0]				

Bit	Name	Attribute	Description
15	NSPEC	R/W	Non-Specific EOI. Set 1: indicates non-specific EOI. Set 0: indicates the specific EOI interrupt type in S[4:0].
14-5	Rsvd	RO	Reserved
4-0	S[4:0]	<del>R/W</del>	Source EOI Type. It specifies the EOI type of the interrupt that is currently being processed.

删除: R/W

## 14. DMA UNIT

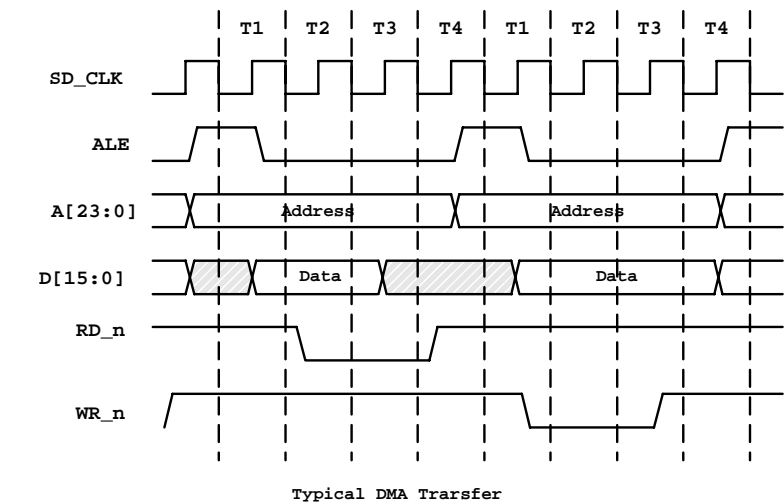
The DMA controller provides the data transfer between the memory and peripherals without the intervention of the CPU. There are two DMA channels in the DMA unit. Each channel can accept DMA requests from one of three sources: external pins (DRQ0 for channel 0 or DRQ1 for channel 1), serial ports (port 0 or port 1), or Timer 2 overflow. The data transfer from sources to destinations can be memory to memory, memory to I/O, I/O to I/O, or I/O to memory. Either bytes or words can be transferred to or from even or odd addresses and two bus cycles are necessary (read from sources and write to destinations) for each data transfer.



### 14.1 DMA Operation

Every DMA transfer consists of two bus cycles (see figure of Typical DMA Transfer) and the two bus cycles cannot be separated by a bus hold request, a refresh request, or another DMA request. The registers (CAh, C8h, C6h, C4h, C2h, C0h, DAh, D8h, D6h, D4h, D2h, and D0h) are used to configure and operate the two DMA channels.





删除:

删除:

Register Offset: CAh (DMA0)  
Register Name: DMA Control Registers  
Reset Value : 0000h

删除: FFF9h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM/IO_n	DDEC	DINC	SM/IO_n	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	EXT	CHG	ST	B_n/W

The definitions of Bit [15:0] for DMA0 are the same as those of Bit [15:0] of Register DAh for DMA1.

Register Offset: C8h (DMA0)  
Register Name: DMA Transfer Count Register  
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	DMA 0 transfer Count. The value of this register will be decremented by 1 after each transfer.

**Register Offset:** C6h (DMA0)  
**Register Name:** DMA Destination Address High Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DDA[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	DDA[23:16]	R/W	High DMA 0 Destination Address. These bits are mapped to A[23:16] during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 00000000b.

**Register Offset:** C4h (DMA0)  
**Register Name:** DMA Destination Address Low Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDA[15:0]															

Bit	Name	Attribute	Description
15-0	DDA[15:0]	R/W	Low DMA 0 Destination Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DDA [23:0] will be incremented or decremented by 2 <u>or</u> 1 after each DMA transfer.

**Register Offset:** C2h (DMA0)  
**Register Name:** DMA Source Address High Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DSA[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	DSA[23:16]	R/W	High DMA 0 Destination Address. These bits are mapped to A[23:16] during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 00000000b.

**Register Offset:** C0h (DMA0)  
**Register Name:** DMA Source Address Low Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSA[15:0]															

Bit	Name	Attribute	Description
15-0	DSA[15:0]	R/W	Low DMA 0 Destination Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DSA [23:0] will be incremented or decremented by 2 <u>or 1</u> after each DMA transfer.

**Register Offset:** DAh (DMA1)  
**Register Name:** DMA Control Registers  
**Reset Value :** 0000h

删除: FFF9h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM/IO_n	DDEC	DINC	DM/IO_n	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	EXT	CHG	ST	B_n/W

Bit	Name	Attribute	Description
15	DM/IO_n	R/W	Destination Address Space Select. Set 1: The destination address is in memory space. Set 0: The destination address is in I/O space.
14	DDEC	R/W	Destination Decrement. Set 1: The destination address is automatically decremented after each transfer. The B_n/W (bit 0) bit determines the decrement value, which is by 1 or 2 when both DDEC and DINC bits are set to 1 <u>or 0</u> . The address remains constant. Set 0: Disable the decrement function.
13	DINC	R/W	Destination Increment. Set 1: The destination address is automatically incremented after each transfer. The B_n/W (bit 0) bit determines the incremented value is by 1 or 2. Set 0: Disable the decrement function.
12	SM/IO_n	R/W	Source Address Space Select. Set 1: The Source address is in memory space. Set 0: The Source address is in I/O space.
11	SDEC	R/W	Source Decrement. Set 1: The Source address is automatically decremented after each transfer. The B_n/W (bit 0) bit determines the decremented value is by 1 or 2 when both SDEC and SINC bits are set to 1 <u>or 0</u> . The address remains constant. Set 0: Disable the decrement function.

10	SINC	R/W	Source Increment. Set 1: The Source address is automatically incremented after each transfer. The B_n/W (bit 0) bit determines the incremented value is by 1 or 2. Set 0: Disable the decrement function.
9	TC	R/W	Terminal Count. Set 1: The synchronized DMA transfer is terminated when the DMA Transfer Count Register reaches 0. Set 0: The synchronized DMA transfer is <u>not</u> terminated when the DMA Transfer Count Register reaches 0. Unsynchronized DMA transfer is always terminated when the DMA transfer count register reaches 0, regardless of the setting of this bit.
8	INT	R/W	Interrupt. Set 1: DMA unit generates an interrupt request when the transfer count is completed. The TC bit must be set to 1 to generate an interrupt.
7-6	SYN[1:0]	R/W	Synchronization Type Selection. <b>SYN1 , SYN0 -- Synchronization Type</b> 0 , 0 -- Unsynchronized 0 , 1 -- Source synchronized 1 , 0 -- Destination synchronized 1 , 1 -- Reserved
5	P	R/W	Priority. Set 1: It selects high priority for this channel when both DMA 0 and DMA 1 are transferred in the same time.
4	TDRQ	R/W	Timer Enable/Disable Request. Set 1: Enable the DMA requests from timer 2. Set 0: Disable the DMA requests from timer 2.
3	<del>EXT</del>	<del>R/W</del>	<del>This bit enables the external interrupt functionality of the corresponding DRQ pin. Set 1: the external pin is an INT pin and requests on the pin are passed to the interrupt controller. Set 0: The pin functions as a DRQ pin.</del>
2	CHG	R/W	Changed Start Bit. This bit must be set to 1 when the ST bit is modified.
1	ST	R/W	Start/Stop DMA channel. Set 1: Start the DMA channel Set 0: Stop the DMA channel
0	B_n/W	R/W	Byte/Word Select. Set 1: The address is incremented or decremented by 2 after each transfer. Set 0: The address is incremented or decremented by 1 after each transfer. <u>Only byte transfer is supported if either source or destination bus width is 8 bit.</u>

刪除: Reserved

刪除: Rsvd

刪除: 0

**Register Offset:** D8h (DMA1)  
**Register Name:** DMA Transfer Control Register  
**Reset Value :** 0000h

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

TC[15:0]

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	DMA 1 transfer Count. The value of this register will be decremented by 1 after each transfer.

**Register Offset:** D6h (DMA1)  
**Register Name:** DMA Destination Address High Register  
**Reset Value :**

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Reserved

DDA[23:16]

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	DDA[23:16]	R/W	High DMA 1 Destination Address. These bits are mapped to A[23:16] during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 00000000b.

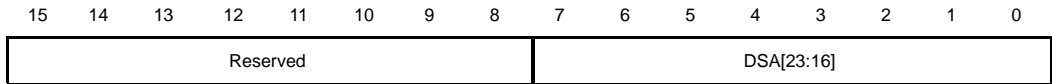
**Register Offset:** D4h (DMA1)  
**Register Name:** DMA Destination Address Low Register  
**Reset Value :**

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

DDA[15:0]

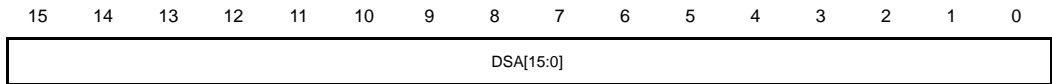
Bit	Name	Attribute	Description
15-0	DDA[15:0]	R/W	Low DMA 1 Destination Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DDA [23:0] will be incremented or decremented by 2 <u>or 1</u> after each DMA transfer.

**Register Offset:** D2h (DMA1)  
**Register Name:** DMA Source Address High Register  
**Reset Value :**



Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	DSA[23:16]	R/W	High DMA 1 Destination Address. These bits are mapped to A[23:16] during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 00000000b.

**Register Offset:** D0h (DMA1)  
**Register Name:** DMA Source Address Low Register  
**Reset Value :**



Bit	Name	Attribute	Description
15-0	DSA[15:0]	R/W	Low DMA 1 Source Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DSA[23:0] will be incremented or decremented by 2 <u>or 1</u> after each DMA transfer.

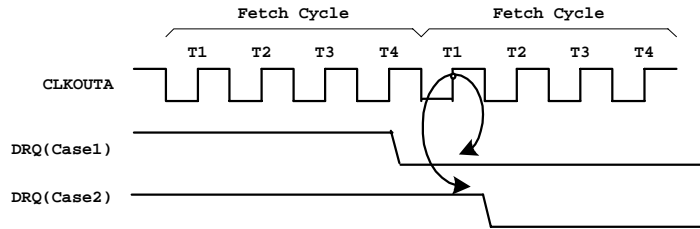
### 14.2 External Requests

External DMA requests are asserted on the DRQ pins. The DRQ pins are sampled on the falling edge of SD\_CLK. It takes a minimum of four clocks before the DMA cycle is initiated by the Bus Interface. The DMA request is cleared four clocks before the end of the DMA cycle. And no DMA acknowledge is provided, since the chip-selects (PCSx\_n) can be programmed to be active for a given block of memory or I/O space, and the DMA source and destination address registers can be programmed to point to the same given block.

DMA transfer can be either source- or destination-synchronized, and it can also be unsynchronized. The Source-Synchronized Transfer figure shows the typical source-synchronized transfer, which provides the source device at least three clock cycles from the time. It is acknowledged to dessert its DRQ line.

刪除: CLKOUTA

刪除: MCSx\_n,

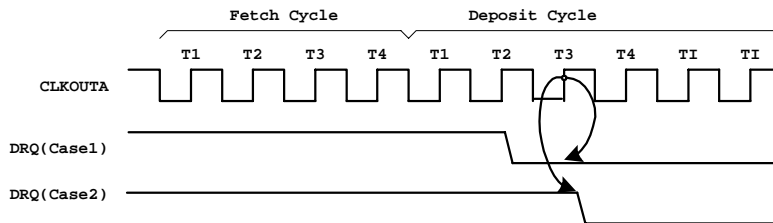


**NOTES:**

- Case1 : Current source synchronized transfer will not be immediately followed by another DMA transfer.
- Case2 : Current source synchronized transfer will be immediately followed by another DMA transfer.

### Source-Synchronized Transfers

The Destination-Synchronized Transfer figure shows the typical destination-synchronized transfer, which differs from a source-synchronized transfer in which two idle states are added to the end of the deposit cycle. The two idle states extend the DMA cycle to allow the destination device to de-assert its DRQ pin four clocks before the end of the cycle. If the two idle states were not inserted, the destination device would not have time to de-assert its DRQ signal.



**NOTES:**

- Case1 : Current destination synchronized transfer will not be immediately followed by another DMA transfer.
- Case2 : Current destination synchronized transfer will be immediately followed by another DMA transfer.

### Destination-Synchronized Transfers

删除:

<sp>

### **14.3    Serial Port/DMA Transfer**

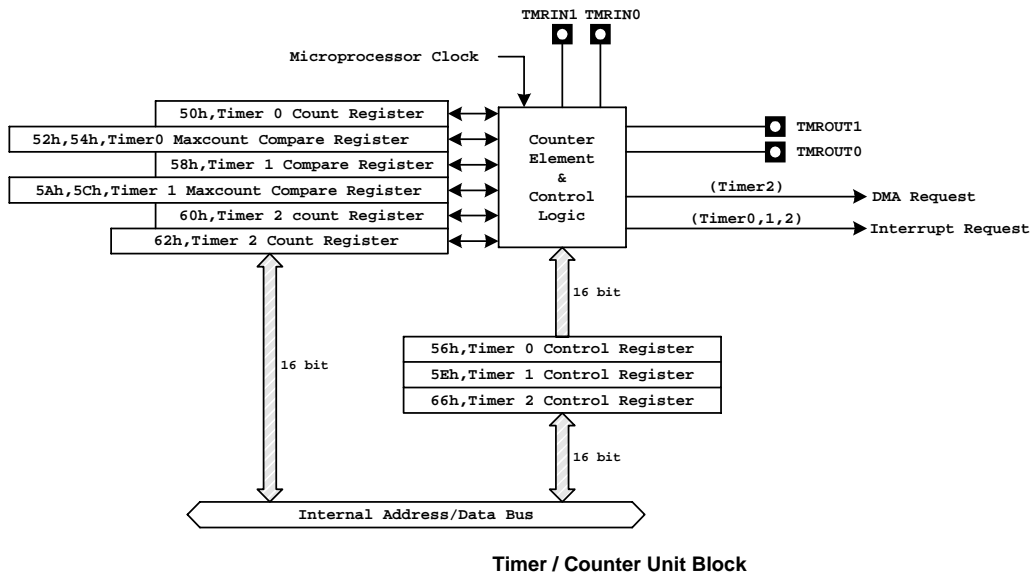
The serial port data can be DMA transfer to or from memory or I/O space. And the B\_n/W bit of the DMA Control Register must be set to 0 for byte transfer. The map address of the Transmit Data Register is written to the DMA Destination Address Register and the memory or I/O address is written to the DMA Source Address Register, when the data are transmitted. The map address of the Receive Data Register is written to the DMA Source Address Register and the memory or I/O address is written to the DMA Destination Address Register, when the data are received.

The software is programmed through the Serial Port Control Register to perform the serial port/ DMA transfer. When a DMA channel is in use by a serial port, the corresponding external DMA request signal is deactivated. For DMA to the serial port, the DMA channel should be configured as being destination-synchronized. For DMA from the serial port, the DMA channel should be configured as source-synchronized.

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## 15. Timer Control UNIT



There are three 16-bit programmable timers in the R2010C. The timer operation is independent of the CPU. These three timers can be programmed as a timer element or as a counter element. Timer 0 and 1 are each connected to two external pins (TMRIN0, TMRIN1, TMRROUT0, TMRROUT1), which can be used to count or time external events, or used to generate variable-duty-cycle waveforms. Timer 2 is not connected any external pins. It can be used as a prescaler to Timer 0 and Timer 1 or as a DMA request source.

**Register Offset:** 56h  
**Register Name:** Timer 0 Mode/Control Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

These bit definitions for timer 0 are the same as those of register 5Eh for timer 1.

**Register Offset:** 50h  
**Register Name:** Timer 0 Count Register  
**Reset Value :**

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

TC[15:0]

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Count Value. This register contains the current count of Timer 0. The count is incremented by one every 8 internal processor clocks, or prescaled by Timer 2, or incremented by one every 8 external clock which is configured the external clock select bit to refer to the TMRIN1 signal.

**Register Offset:** 52h  
**Register Name:** Timer 0 Maxcount Compare A Register  
**Reset Value :**

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

TC[15:0]

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Compare A Value.

**Register Offset:** 54h  
**Register Name:** Timer 0 Maxcount Compare B Register  
**Reset Value :**

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

TC[15:0]

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Compare B Value.

**Register Offset:** 5Eh  
**Register Name:** Timer 1 Mode/Control Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

Bit	Name	Attribute	Description
15	EN	R/W	Enable Bit. Set 1: The timer 1 is enabled. Set 0: The timer 1 is inhibited from counting. The INH_n bit must be set to 1 during writing the EN bit, and the INH_n bit and EN bit must be in the same write.
14	INH_n	R/W	Inhibit Bit. This bit allows selective updating the EN bit. The INH_n bit must be set to 1 during writing the EN bit, and both the INH_n bit and EN bit must be in the same write. This bit is not stored and is always read as 0.
13	INT	R/W	Interrupt Bit. Set 1: An interrupt request is generated when the count register equals a maximum count. If the timer is configured in dual max-count mode, an interrupt is generated each time the count reaches Max-Count A or Max-Count B. Set 0: Timer 1 will not issue interrupt request.
12	RIU	R/W	Register in Use Bit. Set 1: The Maxcount Compare B Register of timer 1 is being used. Set 0: The Maxcount Compare A Register of timer 1 is being used.
11-6	Rsvd	RO	Reserved
5	MC	R/W	Maximum Count Bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. In dual maxcount mode, this bit is set as each time either Maxcount Compare A or Maxcount Compare B register is reached. This bit is set regardless of the EN bit (offset 5Eh [15]).
4	RTG	R/W	Re-trigger Bit. This bit defines the control function by the input signal of TMRIN1 pin. When EXT=1 (5Eh.2), this bit is ignored. Set 1: Timer1 Count Register (58h) counts internal events; Reset the counting on every TMRIN1 input signal going from low to high (rising edge trigger). Set 0: Low input holds the timer 1 Count Register (58h) value; High input enables the counting which counts the internal events. <b>The definition of setting the (EXT, RTG)</b> (0, 0) – Timer1 counts the internal events. If the TMRIN1 pin remains high. (0, 1) – Timer1 counts the internal events; count register resets on every rising transition on the TMRIN1 pin. (1, x) – TMRIN1 pin input acts as a clock source and timer1 count register is incremented by one every 8 external clocks.
3	P	R/W	Prescalar Bit. This bit and EXT bit (5Eh [2]) define the timer 1 clock source. <b>The definition of setting the (EXT, P)</b> (0, 0) – Timer1 Count Register is incremented by one every 8 internal processor clocks. (0, 1) – Timer1 Count Register is incremented by one which is prescaled by Timer 2. (1, x) – TMRIN1 pin input acts as a clock source and Timer1 Count Register is incremented by one every 8 external clocks.

删除: 66

2	EXT	R/W	External Clock Bit. Set 1: Timer 1 clock source from external. Set 0: Timer 1 clock source from internal.
1	ALT	R/W	Alternate Compare Bit. This bit controls whether the timer runs in single or dual maximum count mode. Set 1: Specify dual maximum count mode. In this mode, the timer counts to Maxcount Compare A, then resets the count register to 0. The timer counts to Maxcount Compare B, then resets the count register to 0 again, and starts over with Maxcount Compare A. Set 0: Specify single maximum count mode. In this mode, the timer counts to the value contained in Maxcount Compare A and reset to 0, and then the timer counts to Maxcount Compare A again. Maxcount Compare B is not used in this mode.
0	CONT	R/W	Continuous Mode Bit. Set 1: The timer runs continuously. Set 0: The timer will halt after each counting to the maximum count and EN bit will be cleared.

**Register Offset:** 58h  
**Register Name:** Timer 1 Count Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Count Value. This register contains the current count of timer 1. The count is incremented by one every 8 internal processor clocks, prescaled by Timer 2, or incremented by one every 8 external clocks which is configured as the external clock select bit to refer to the TMRIN1 signal.

**Register Offset:** 5Ah  
**Register Name:** Timer 1 Maxcount Compare A Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Compare A Value.

**Register Offset:** 5Ch  
**Register Name:** Timer 1 Maxcount Compare B Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

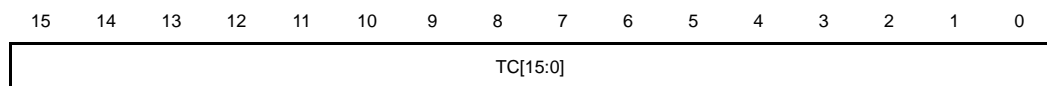
Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Compare B Value.

**Register Offset:** 66h  
**Register Name:** Timer 2 Mode/Control Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	0	0	0	0	0	0	0	MC	0	0	0	0	CONT

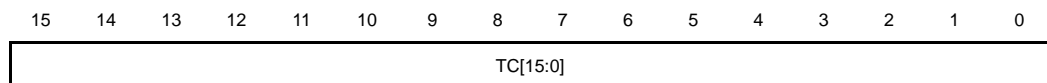
Bit	Name	Attribute	Description
15	EN	R/W	Enable Bit. Set 1: Timer 2 is enabled. Set 0: Timer 2 is inhibited from counting. The INH_n bit must be set to 1 during writing the EN bit, and the INH_n and EN bit must be in the same write.
14	INH_n	R/W	Inhibit Bit. This bit allows selective updating the EN bit. The INH_n bit must be set to 1 during writing the EN bit, and both the INH_n and EN bit must be in the same write. This bit is not stored and is always read as 0.
13	INT	R/W	Interrupt Bit. Set 1: An interrupt request is generated when the count register equals a maximum count. Set 0: Timer 2 will not issue interrupt request.
12-6	Rsvd	RO	Reserved
5	MC	R/W	Maximum Count Bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. This bit is set regardless of the EN bit (66h.15).
4-1	Rsvd	RO	Reserved
0	CONT	R/W	Continuous Mode Bit. Set 1: The timer is continuously running when it reaches the maximum count. Set 0: The EN bit (66h [15]) is cleared and the timer is held after each timer count reaches the maximum count.

**Register Offset:** 60h  
**Register Name:** Timer 2 Count Register  
**Reset Value :**



Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 2 Count Value. This register contains the current count of Timer 2. The count is incremented by one every 8 internal processor clocks.

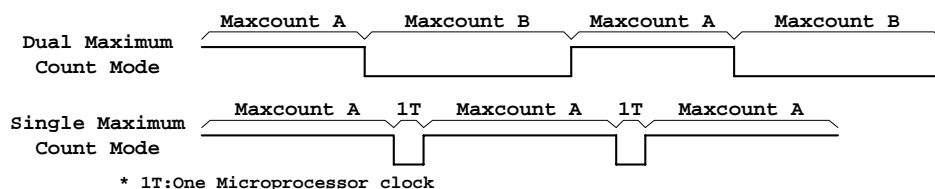
**Register Offset:** 62h  
**Register Name:** Timer 2 Maxcount Compare A Register  
**Reset Value :**



Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 2 Compare A Value.

## 15.1 Timer/Counter Unit Output Mode

Timers 0 and 1 can use one maximum count value or two maximum count values. Timer 2 can use only one maximum count value. Timer 0 and Timer1 can be configured to be a single or dual maximum count mode, the TMROUT0 or TMROUT1 signals can be used to generate waveforms of various duty cycles.



**Timer/Counter Unit Output Modes**

## 15.2 Watchdog Timer

The R2010C has one independent watchdog timer, which is programmable. **The watchdog timer is active after reset** and the timeout count with a maximum count value. The keyed sequence (3333h, CCCCh) must be written to the register (E6h) first, then the new configuration to the Watchdog Timer Control Register. It is a single write, so every writing to the Watchdog Timer Control Register will follow this rule.

When the watchdog timer activates, an internal counter is counting. If this internal count is over the watchdog timer duration, the watchdog timeout happens. The keyed sequence (AAAAh, 5555h) must be written to the register (E6h) to reset the internal count and prevent the watchdog timeout. The internal count should be reset before the Watchdog Timer timeout period is modified to ensure that an immediate timeout will not occur.

Register Offset: E6h  
Register Name: Watchdog Timer Control Register  
Reset Value : C080h

删除: 60h

删除: Timer 2 Count  
Register

删除:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENA	WRST	RSTFLAG	NMIFLAG	Rsvd				COUNT							

Bit	Name	Attribute	Description
15	ENA	R/W	Enable Watchdog Timer. Set 1: Enable Watchdog Timer. Set 0: Disable Watchdog Timer.
14	WRST	R/W	Watchdog Reset. Set 1: WDT generates a system reset when WDT timeout count is reached. Set 0: WDT generates an NMI interrupt when WDT timeout count is reached if the NMIFLAG bit is 0. If the NMIFLAG bit is 1, the WDT will generate a system reset when timeout.
13	RSTFLAG	R/W	Reset Flag. When watchdog timer reset event has occurred, hardware will set this bit to 1. This bit will be cleared by any keyed sequence write to this register or external reset. This bit is 0 after an external reset or 1 after a watchdog timer reset.
12	NMIFLAG	R/W	NMI Flag. After WDT generates an NMI interrupt, this bit will be set to 1 by H/W. This bit will be cleared by any keyed sequence written to this register.
11-8	Rsvd	RO	Reserved

7-0	COUNT	R/W	Timeout Count. The COUNT setting determines the duration of the watchdog timer timeout interval.  a.The duration equation: <b>Duration</b> =(2 <sup>Exponent</sup> ) / (Frequency/2) b.The Exponent of the COUNT setting: (Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2, Bit 1, Bit 0) = (Exponent) ( 0 , 0 , 0 , 0 , 0 , 0 , 0 , 0 ) = (N/A) ( x , x , x , x , x , x , x , 1 ) = ( 10 ) ( x , x , x , x , x , x , 1 , 0 ) = ( 20 ) ( x , x , x , x , x , 1 , 0 , 0 ) = ( 21 ) ( x , x , x , x , 1 , 0 , 0 , 0 ) = ( 22 ) ( x , x , x , 1 , 0 , 0 , 0 , 0 ) = ( 23 ) ( x , x , 1 , 0 , 0 , 0 , 0 , 0 ) = ( 24 ) ( x , 1 , 0 , 0 , 0 , 0 , 0 , 0 ) = ( 25 ) ( 1 , 0 , 0 , 0 , 0 , 0 , 0 , 0 ) = ( 26 )  c. Watchdog timer Duration reference table: For example: System clock =100Mhz and frequency exponent=10, then Duration = 2 <sup>10</sup> / ( 100Mhz / 2 ) = 2048 / 100Mhz = 20.48 us								
			Frequency\ Exponent	10	20	21	22	23	24	25	26
			75 MHz	27.3 us	28 ms	55.9 ms	111.8 ms	223.7 ms	447.4 ms	894.8 ms	1.79 s
			100 MHz	20.5 us	21 ms	41.9 ms	83.9 ms	167.8 ms	335.5 ms	671 ms	1.34 s

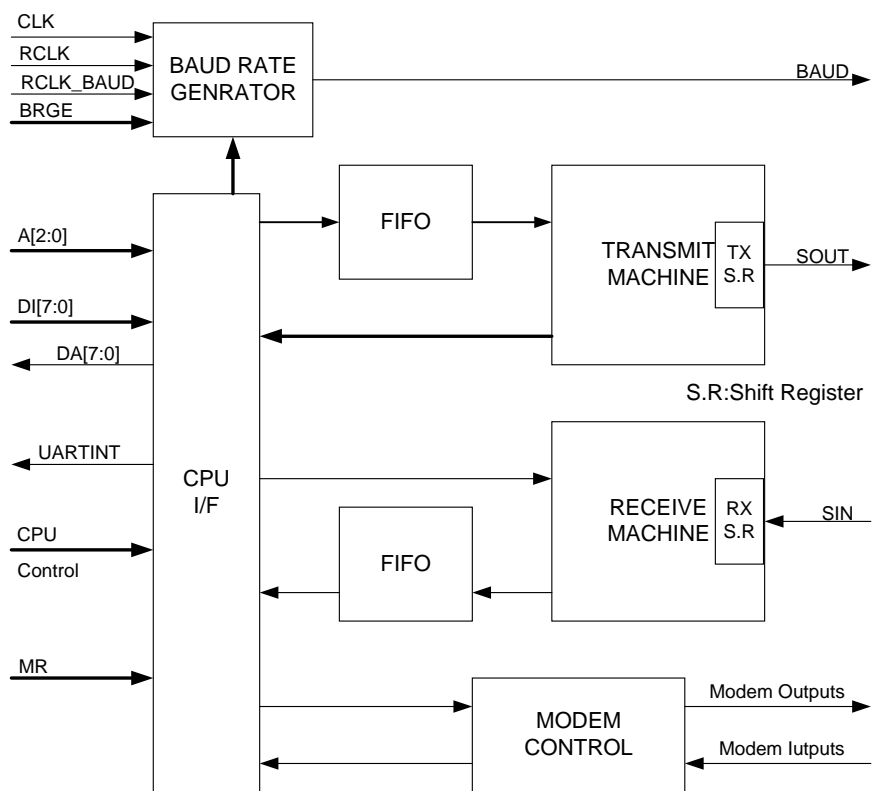


## 16. 16550 UART Serial Port

The system programmer may access any of the UART registers summarized in the following Table via the CPU. These registers control the UART operation in which the transmission and reception of data and status are included, and each register bit in the Table has its own name.

Register Address	Register Name	Mnem.	Bit No.									Note.
			15-8	7	6	5	4	3	2	1	0	
80h/10h	Receiver Buffer Register	<b>RBR</b>	0	RBR[7]	RBR[6]	RBR[5]	RBR[4]	RBR[3]	RBR[2]	RBR[1]	RBR[0]	DLAB=0 & read only
	Transmitter Holding Register	<b>THR</b>	0	THR[7]	THR[6]	THR[5]	THR[4]	THR[3]	THR[2]	THR[1]	THR[0]	DLAB=0 & write only
	Divisor Latch(LS)	<b>DLL</b>	0	DL[7]	DL[6]	DL[4]	DL[4]	DL[3]	DL[2]	DL[1]	DL[0]	DLAB=1
82h/12h	Interrupt Enable Register	<b>IER</b>	0	0	0	0	0	EMSI	ERLSI	ETHREI	ERDAI	DLAB=0
	Divisor Latch(MS)	<b>DLM</b>	0	DL[15]	DL[14]	DL[13]	DL[12]	DL[11]	DL[10]	DL[9]	DL[8]	DLAB=1
84h/14h	Interrupt Identified Register	<b>IIR</b>	0	FIFO Enabled (Note)	FIFO Enabled (Note)	0	0	IID[2]	IID[1]	IID[0]	IP	Read Only
	FIFO Control Register	<b>FCR</b>	DMAC TL2-0	RCVR Trigger Level (MSB)	RCVR Trigger Level (LSB)	Reserved	Reserved	DMA Mode Select	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enabled	Write Only
86h/16h	Line Control Register	<b>LCR</b>	0	DLAB	SB	SP	EPS	PEN	STB	WLS[1]	WLS[0]	
88h/18h	MODEM Control Register	<b>MCR</b>	0	0	0	ACE	Loop	<u>LD</u> CD	<u>L</u> R	RTS	DTR	
8Ah/1Ah	Line Status Register	<b>LSR</b>	0	Error in RCVR FIFO (Note)	TEMT	THRE	BI	FE	PE	OE	DR	
8Ch/1Ch	MODEM Status Register	<b>MSR</b>	0	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS	
8Eh/1Eh	Scratch Register	<b>SCR</b>	0	SCR[7]	SCR[6]	SCR[5]	SCR[4]	SCR[3]	SCR[2]	SCR[1]	SCR[0]	

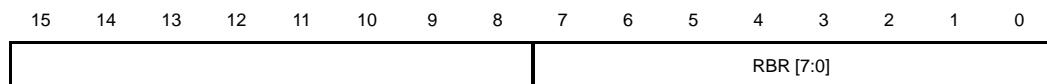
Note: These bits are always 0 in the 16450 mode.



UART Block Diagram

## 16.1 Receiver Buffer Register and Transmitter Holding Register

**Register Offset:** 80h  
**Register Name:** UART0 Receiver Buffer Register  
**Reset Value :**



This register is Receiver Buffer Register when DLAB=0 and the read function is operated.

**Register Offset:** 80h  
**Register Name:** UART0 Transmitter Holding Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								THR [7:0]							

This register is Transmitter Holding Register when DLAB=0 and the write function is operated.

## 16.2 Divisor Latch LS and MS Register

The divisor value, DLL[15:0], is the host clock / 16 / Baud Rate.

For example:

Host Clock=75Mhz, and Baud Rate=57600, then

Divisor=75Mhz/16/57600=81.3 → 81

**Register Offset:** 80h  
**Register Name:** UART0 Divisor Latch (LS) Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DLL [7:0]							

This register is Divisor Latch (LS) Register when DLAB=1.

**Register Offset:** 82h  
**Register Name:** UART0 Divisor Latch (MS) Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DLL [15:8]							

This register is Divisor Latch (MS) Register when DLAB=1.

### 16.3 Interrupt Enable Register

This Interrupt Enable Register (IER) enables the four types of UART interrupts. Each interrupt can individually activate the interrupt output signal (UARTINT). It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, setting the relative bit of the IER register to 1 will enable the selected interrupt(s). Disabling an interrupt prevents it from being indicated as being active in the IIR and from activating the UARTINT output signal. All other system functions operate in their normal manners, including the setting of the Line Status and MODEM Status Registers. The details of each bit of the IER are described as below:

**Register Offset:** 82h  
**Register Name:** UART0 Interrupt Enable Register  
**Reset Value :** XX00h

刪除: five

刪除:

刪除: R

刪除: R

刪除:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	BMSI	ERLSI	ETHREI	ERDAI

Bit	Name	Attribute	Description
7-4	Rsvd	RO	Reserved and always 0.
3	EMSI	R/W	The MODEM Status Interrupt bit. Set to 1 to enable the MODEM Status Interrupt.
2	ERLSI	R/W	The Enable Receiver Line Status Interrupt bit. Set to 1 to enable the Receiver Line Status Interrupt.
1	ETHREI	R/W	The Enable Transmitter Holding Register Empty Interrupt bit. Set to 1 to enable the Transmitter Holding Register Empty Interrupt.
0	ERDAI	R/W	The Enable Received Data Interrupt bit. Set to 1 to enable the Received Data Available Interrupt (and timeout interrupts in the FIFO mode).

### 16.4 Interrupt Identification Register

This is a read only register. In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the Interrupt Identification Register (IIR). The four levels of interrupt conditions in priority order are Receiver Line Status, Received Data Ready, Transmitter Holding Register Empty, and MODEM Status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. The details of each bit of Interrupt Identification Register are described as below.

**Register Offset:** 84h  
**Register Name:** UART0 Interrupt Identified. Register (Read Only)  
**Reset Value :** ~~XX01h~~

删除:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								FIFOs Enabled	FIFOs Enabled	0	0	IID2	IID1	IID0	IP

Bit	Name	Attribute	Description
7-6	FIFOs Enabled	R/W	These two bits are set when FCR [0]=1.
5-4	Rsvd	RO	Reserved and always 0.
3	IID2	R/W	The Interrupt ID indicator. In the NS16450 Mode, this bit is 0. In the FIFO mode, this bit is set along with bit 2 when a timeout interrupt is pending.
2-1	IID[1:0]	R/W	The Interrupt ID indicator. These two bits are used to identify the highest priority interrupt pending as indicated in the following table:
0	IP	R/W	The Interrupt Pending indicator. This bit can be used in a prioritized interrupt environment to indicate whether an interrupt is pending or not. Set 1: Indicate that no interrupt is pending. Set 0: Indicate that an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.

#### Interrupt Control Function:

FIFO Mode Only		Interrupt Identification Register		Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Rest Control
0	0	0	1		None	none	
0	1	1	0	Highest	Receiver Line Status	overrun error, parity error, framing error, or break interrupt	reading the line status register
0	1	0	0	Second	Received Data Available	received data available or trigger level reached	reading the receiver buffer register or the FIFO dropping below the trigger level
1	1	0	0	Second	Character Timeout Indication	no character has been removed from or input to the RCVR FIFO during the last 4 characters times and there is at least 1 character in it during this time	reading the receiver buffer register
0	0	1	0	Third	Transmitter Holding Register Empty	transmitter holding register empty	reading the IIR register (if the source of interrupt is available) or writing into the transmitter holding register
0	0	0	0	Fourth	MODEM Status	clear to send, data set	reading the modem status

删除: TT

						ready, ring indicator, or data carrier detect	register
--	--	--	--	--	--	---	----------

## 16.5 FIFO Control Register

The FIFO Control Register (write only) is at the same location as the Interrupt Identification Register (read only). This register is used to enable the FIFO, clear the FIFO, set the RCVR FIFO trigger level, and select the type of DMA signaling.

**Register Offset:** 84h  
**Register Name:** UART0 FIFO Control Register (Write Only)  
**Reset Value :** 0x000h

删除:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						DMACTL[2:0]		RCVR Trigger (MSB)	RCVR Trigger (LSB)	Rsvd		DMA Mode Select	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enabled

Bit	Name	Attribute	Description																											
10-8	DMACTL [2:0]	R/W	<div>With the DMA transfers listed as follows, users can configure these bits for the UART Port.</div> <table><thead><tr><th><u>DMACTL [2:0]</u></th><th><u>Receive</u></th><th><u>Transmit</u></th></tr></thead><tbody><tr><td>000</td><td>No DMA</td><td>No DMA</td></tr><tr><td>001</td><td>DMA0</td><td>DMA1</td></tr><tr><td>010</td><td>DMA1</td><td>DMA0</td></tr><tr><td>011</td><td>Reserved</td><td>Reserved</td></tr><tr><td>100</td><td>DMA0</td><td>No DMA</td></tr><tr><td>101</td><td>DMA1</td><td>No DMA</td></tr><tr><td>110</td><td>No DMA</td><td>DMA0</td></tr><tr><td>111</td><td>No DMA</td><td>DMA1</td></tr></tbody></table>	<u>DMACTL [2:0]</u>	<u>Receive</u>	<u>Transmit</u>	000	No DMA	No DMA	001	DMA0	DMA1	010	DMA1	DMA0	011	Reserved	Reserved	100	DMA0	No DMA	101	DMA1	No DMA	110	No DMA	DMA0	111	No DMA	DMA1
<u>DMACTL [2:0]</u>	<u>Receive</u>	<u>Transmit</u>																												
000	No DMA	No DMA																												
001	DMA0	DMA1																												
010	DMA1	DMA0																												
011	Reserved	Reserved																												
100	DMA0	No DMA																												
101	DMA1	No DMA																												
110	No DMA	DMA0																												
111	No DMA	DMA1																												
7-6	RCVRTL [1:0]	R/W	<div>RCVR Trigger.</div> <div>These two bits are used to set the trigger level for the RCVR FIFO interrupt.</div> <table><thead><tr><th colspan="2"><b>RCVRTL[1:0] – RCVR FIFO Trigger Level (Bytes)</b></th></tr></thead><tbody><tr><td>0 0</td><td>-- 01 Bytes</td></tr><tr><td>0 1</td><td>-- 04 Bytes</td></tr><tr><td>1 0</td><td>-- 08 Bytes</td></tr><tr><td>1 1</td><td>-- 14 Bytes</td></tr></tbody></table>	<b>RCVRTL[1:0] – RCVR FIFO Trigger Level (Bytes)</b>		0 0	-- 01 Bytes	0 1	-- 04 Bytes	1 0	-- 08 Bytes	1 1	-- 14 Bytes																	
<b>RCVRTL[1:0] – RCVR FIFO Trigger Level (Bytes)</b>																														
0 0	-- 01 Bytes																													
0 1	-- 04 Bytes																													
1 0	-- 08 Bytes																													
1 1	-- 14 Bytes																													
5-4	Rsvd	RO	Reserved																											
3	DMA Mode Select	R/W	<div>DMA Mode Select.</div> <div>Setting FCR0[3]=1 will cause the <u>UART</u> to change from mode 0 to mode 1 if FCR0[0]=0.</div>																											
2	XMIT FIFO Reset	R/W	<div>XMIT FIFO Reset. Writing a 1 to FCR0[2] clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.</div>																											
1	RCVR	R/W	<div>RCVR FIFO Reset.</div>																											

刪除: RXRDY and TXRDY pins

**刪除:** (see description of RXRDY and TXRDY pins)

	FIFO Reset		Writing a 1 to FCR0[1] clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.
0	FIFO Enabled	R/W	FIFO Enable. Writing a 1 to FCR0 enables both the XMIT and RCVR FIFO. Resetting FCR0[0] will clear all bytes in both FIFO. When changing from FIFO Mode to NS16450 Mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when <u>written to</u> other FCR bits or they will not be programmed.

删除: are written to

## 16.6 Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The detailed contents of each bit of LCR register is as follows:

**Register Offset:** 86h  
**Register Name:** UART0 Line Control Register  
**Reset Value :** XX00h

删除:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DLAB	Set Break	Stick Parity	EPS	PEN	STB	WSL1	WSL0

Bit	Name	Attribute	Description
7	DLAB	RW	Divisor Latch Access bit. Set 1: To access the Divisor Latches of the Baud Generator during a Read or Write operation. Set 0: To access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register
6	SB	R/W	Break Control bit. It causes a break condition to be transmitted to the receiving UART. Set 1: the serial output (SOUT) is forced to the Spacing (logic 0) state. Set 0: the Break is disabled. The Break Control bit acts only on SOUT and has no effect on the transmitter logic. <b>Note:</b> This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break. 1. Load an all Os, pad character, in response to THRE. 2. Set break after the next THRE. 3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal

			<i>transmission has to be restored.</i> <i>During the break, the Transmitter can be used as a character timer to accurately establish the break duration.</i>
5	SP	R/W	Stick Parity bit. Set Bit 5=1, Bit 4=1, & Bit 3=1, the Parity bit is transmitted and checked as logic 0. Set Bit 5=1, Bit 4=0, & Bit 3=1, the Parity bit is transmitted and checked as logic 1. Set Bit 5=0, Stick Parity is disabled.
4	EPS	R/W	Even Parity Select bit. Set Bit 4=0 & Bit 3=1, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. Set Bit 4=1 & Bit 3=1, an even number of logic 1s is transmitted or checked.
3	PEN	R/W	Parity Enable bit. Set 1: A Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)
2	STB	R/W	Stop bit. This bit specifies the number of Stop bits transmitted and received in each serial character. Set 0: One Stop bit is generated in the transmitted data. Set 1: One and a half stop bits are generated for a 5-bit word length characters. Two stop bits are generated for 6-, 7-, or 8-bit word length characters. The receiver checks the first Stop bit only, regardless of the number of Stop bits selected.
1-0	WLS[1:0]	R/W	These two specify the number of bits in each transmitted or received serial character. <b>WLS[1:0] -- Character Length</b> 0 0 -- 5-bit character 0 1 -- 6-bit character 1 0 -- 7-bit character 1 1 -- 8-bit character

## 16.7 Modem Control Register

This Modem Control Register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The details are described as below:

**Register Offset:** 88h  
**Register Name:** UART0 MODEM Control Register  
**Reset Value :** ~~XX00h~~

刪除:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	ACE	Loop	LD CD	LRI	RTS	DTR



Bit	Name	Attribute	Description		
7-6	Rsvd	RO	Reserved and always 0.		
5	ACE	R/W	Autoflow Control is Enabled when set. ACE can be configured by MCR bits 1 and 5 as shown in the following table.		
			MCR bit5(AFE)	MCR bit1(RTS)	
			1	1	Auto-RTS and auto-CTS enabled
			1	0	Auto-CTS enabled
			0	X	AFE disabled
4	Loop	R/W	<p>This bit provides a local loop back feature for diagnostic testing of the UART. Set to 1, the following occur: The transmitter Serial Output (SOUT) is set to the Marking (logic 1) state. The receiver Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is “looped back” into the Receiver Shift Register input. The four MODEM Control inputs (CTS_n, DSR_n, RI_n, and DCD_n) are disconnected, and the 2 MODEM Control outputs (DTR_n and RTS_n) are internally connected to the <u>two</u> MODEM Control inputs (<u>DSR_n, CTS_n</u>), and the MODEM Control output pins are forced to their inactive state (high).</p> <p>In the diagnostic mode, data transmitted are immediately received. This feature allows the processor to verify the transmitted and received data paths of the UART.</p> <p>In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the sources of the interrupts are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.</p>		
3, 2	<u>LD</u> <u>CD</u> , <u>L</u> <u>R</u> <u>I</u>	<u>R</u> <u>W</u>	<p><u>Bit3: The bit controls DCD_n signal internal if loop back mode is enabled.</u> <u>Bit2: The bit controls RI_n signal internal if loop back mode is enabled.</u></p>		
1	RTS	R/W	<p>The Request To Send bit. This bit controls the Request To Send (RTS_n) output. Set 1: the RTS_n output is forced to logic 0. Set 0: the RTS_n output is forced to logic 1.</p>		
0	DTR	R/W	<p>The Data Terminal Ready indicator. This bit controls the Data Terminal Ready (DTR_n) output. Set 1: the DTR_n output is forced to logic 0. Set 0: the DTR_n output is forced to logic 1.</p> <p><b>Note:</b> The DTR_n output of the UART may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.</p>		

删除: four

删除: Their sources are external to the part.

删除: 0

## 16.8 Line Status Register

This register provides status information to the part of the CPU processing data transfer. The contents of each Bit of the Line Status Register are described as below.

**Register Offset:** 8Ah  
**Register Name:** UART0 Line Status Register  
**Reset Value :** ~~XX60h~~

刪除:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								Error in RCVR (Note 2)	TEMT	THRE	BI	FE	PE	OE	DR

Bit	Name	Attribute	Description
7	Error in RCVR (Note 2)	R/W	<p>Error in Receive FIFO.</p> <p>In the NS16450 Mode, this is a 0. In the FIFO mode, LSR [7] is set to 1 when there is at least one parity error, framing error or break indication in the FIFO. LSR [7] is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.</p> <p><b>Note:</b> The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.</p>
6	TEMT	R/W	<p>The Transmitter Empty indicator.</p> <p>Set 1: This bit is set to 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty.</p> <p>Set 0: This bit is reset to 0 whenever either the Transmitter Holding Register or the Transmitter Shift Register contains a data character.</p> <p>In the FIFO mode, this bit is set to one whenever the transmitter FIFO and shift register are both empty.</p>
5	THRE	R/W	<p>The Transmitter Holding Register Empty indicator.</p> <p>This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt Enable is set high.</p> <p>Set 1: This bit will be set to 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register.</p> <p>Set 0: This bit is reset to 0 upon the CPU loading character to the Transmitter Holding Register.</p> <p>In the FIFO mode, this bit is set when the XMIT FIFO is empty; it is cleared when at least 1 byte is written to the XMIT FIFO.</p>
4	BI	R/W	<p>Break Interrupt indicator.</p> <p>Set 1: This bit will be set to 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + Data Bits + Parity Bit + Stop Bit).</p> <p>Set 0: This bit will be reset whenever the CPU reads the contents of the Line Status Register.</p> <p>In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs, only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.</p> <p><b>Note:</b> Bits 1 through 4 are the error conditions that produce a Receiver Line Status</p>

			<i>interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.</i>
3	FE	R/W	<p>Framing Error indicator.</p> <p>This bit indicates that the received characters don't have a valid Stop Bit.</p> <p>Set 1: This bit will be set to 1 whenever the Stop Bit follows the last data bit or Parity bit is detected as a logic 0 bit (Spacing level).</p> <p>Set 0: Automatic set to 0 whenever the CPU reads the contents of the Line Status Register.</p> <p>In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error occurs. To do this, it assumes that the framing error was due to the next start bit, so it samples this "start" bit twice and then takes in the "data".</p>
2	PE	R/W	<p>Parity Error indicator.</p> <p>This bit indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity select bit.</p> <p>Set 1: This bit will be set upon detection of a parity error.</p> <p>Set 0: Automatic set to 0 whenever the CPU reads the contents of the Line Status Register.</p> <p>In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.</p>
1	OE	R/W	<p>Overrun Error indicator.</p> <p>This bit indicates that the data in the Receiver Buffer Register were not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character.</p> <p>Set 1: Indicate OE indicator is set to logic 1 upon detection of an overrun condition.</p> <p>Set 0: Automatic reset to 0 whenever the CPU reads the contents of the Line Status Register.</p> <p>If the data in the FIFO mode continue to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.</p>
0	DR	R/W	<p>Data Ready indicator.</p> <p>Set 1: Indicate whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO.</p> <p>Set 0: Automatic set to 0 by reading all of the data in the Receiver Buffer Register or the FIFO.</p>

删除: e

## 16.9 Modem Status Register

This Modem Status Register (MSR) provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to logic 1 whenever a control input from the MODEM changes its state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register. The contents of the MSR register are described as below.

**Register Offset:** 8C  
**Register Name:** UART0 MODEM Status Register  
**Reset Value :** ~~XXX0h~~

删除:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

Bit	Name	Attribute	Description
7	DCD	R/W	Data Carrier Detect. This bit is the complement of the Data Carrier Detect (DCD_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to OUT2 in the MCR.
6	RI	R/W	Ring Indicator. This bit is the complement of the Ring Indicator (RI_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to OUT1 in the MCR.
5	DSR	R/W	Data Set Ready. This bit is the complement of the Data Set Ready (DSR_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to DTR in the MCR.
4	CTS	R/W	Clear To Send. This bit is the complement of the Clear to Send (CTS_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to RTS in the MCR.
3	DDCD	R/W	Delta Data Carrier Detect. This bit indicates that the DCD_n input has changed the state. <b>Note:</b> Whenever bit 0, 1, 2 or 3 is set to logic 1, a MODEM Status Interrupt is generated.
2	TERI	R/W	Trailing Edge Ring Indicator. This bit indicates that the RI_n input has changed from a low to a high state.
1	DDSR	R/W	Delta Data Set Ready. This bit indicates that the DSR_n input has changed the state since the last time it was read by the CPU.
0	DCTS	R/W	Delta <del>Clear To Send</del> . This bit indicates that the CTS_n input has changed the state since the last time it was read by the CPU.

删除: Data Ready

### 16.10 Scratchpad Register

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

**Register Offset:** 8E  
**Register Name:** UART0 Scratch Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								SCR[7:0]							

### 16.11 Programmable Baud Generator

The UART contains a programmable Baud Generator that is divided by any divisor from 2 to  $2^{16}-1$ . The output frequency of the Baud Generator is 16 times the Baud [divisor # = (CPU frequency)/(baud rate\*16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Baud Rates	CPUCLK=75MHz				CPUCLK=100MHz			
	DLM	DLL	Baud	Dev.(%)	DLM	DLL	Baud	Dev.(%)
1200	0Fh	42h	1200	0	14h	58h	1200	0
2400	07h	A1h	2400	0	0Ah	2Ch	2400	0
4800	03h	D1h	4798	0.04	05h	16h	4800	0
9600	01h	E8h	9606	0.06	02h	8Bh	9601	0
19200	0h	F4h	19211	0.06	01h	46h	19171	0.15
38400	0h	7Ah	38422	0.06	0h	A3h	38344	0.15
57600	0h	51h	57870	0.5	0h	6Dh	57339	0.45
115200	0h	29h	114329	0.76	0h	36h	115741	0.47
230400	0h	14h	234375	1.73	0h	1Bh	231481	0.47
460800	0h	0Ah	468750	1.71	0h	0Eh	446428	3.13

删除: capable of taking any clock input from DC to 8.0 MHz and

删除: 4 MHz is the highest input clock frequency recommended when the divisor = 1

删除: -

删除: input

### 16.12 FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR [0]=1, IER [0]=1), RCVR interrupt will occur as follows:

删除: C

- The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

- B. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.
- C. The receiver line status interrupt (IIR=06), as before, has higher priority than the received data available (IIR=04) interrupt.
- D. The data ready bit (LSR [0]) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

- A. A FIFO timeout interrupt will occur, if the following conditions exist:
  - at least one character is in the FIFO.
  - the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
  - the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 ms at 300 BAUD with a 12-bit character.
- B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
- C. When a timeout interrupt has occurred: It is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.
- D. When a timeout interrupt has not occurred: The timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR [0]=1, IER [1]=1), XMIT interrupts will occur as follows:

- A. The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
  - B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE=1. The first transmitter interrupt after changing FCR0 will be immediate, if it is enabled.
- Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

### **16.13 FIFO Polled Mode Operation**

With FCR [0]=1, resetting IER [0], IER [1], IER [2], IER [3] or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMITTER status via the LSR. As stated previously:

LSR [0] will be set as long as there is one byte in the RCVR FIFO.

LSR [1] to LSR [4] will specify which error(s) has occurred.

Character error status is handled the same way as in the interrupt mode, the IIR is not affected since IER2=0.

LSR [5] will indicate when the XMIT FIFO is empty.

LSR [6] will indicate that both the XMIT FIFO and Shift Register are empty.

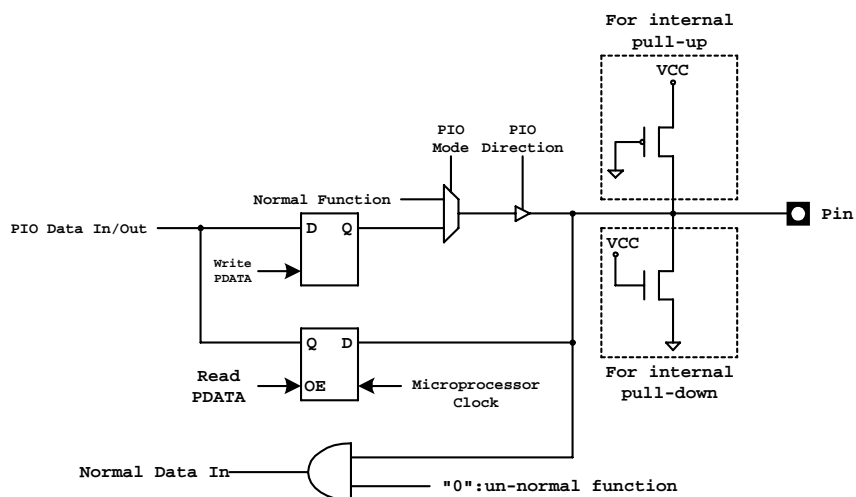
LSR [7] will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

---

## 17. PIO UNIT

The R2010C provides 11 programmable I/O signals, which are multi-functional pins with other signals of normal functions. Software must be used to configure these multi-functional pins as PIO or normal functions by means of programming through these registers (7Ah, 78h, 76h, 74h, 72h, and 70h).



PIO pin Operation Diagram

### 17.1 PIO Multi-Function Pin List Table

PIO No.	Pin No.(PQFP)	Multi Function	Reset status/PIO internal resister
0	8	TMRIN1/SA10	PIO/ Input with 75K pull-up
1	10	TMROUT1/SA8	PIO/ Input with 75K pull-down
3	125	PCS5_n	PIO/ Input with 75K pull-up
10	11	TMROUT0/SA7	PIO/ Input with 75K pull-down
11	9	TMRIN0/SA9	PIO/ Input with 75K pull-up
12	13	DRQ0/INT5/SA5	PIO/ Input with 75K pull-up
13	12	DRQ1/INT6/SA6	PIO/ Input with 75K pull-up
14	126	PCS0_n	PIO/ Input with 75K pull-up
25	33	PCS2_n/IOR_n	PIO/ Input with 75K pull-up
26	34	PCS3_n/IOW_n	PIO/ Input with 75K pull-up
31	4	INT2	PIO/ Input with 75K pull-up

删除: 1

PIO Mode	PIO Direction	Pin Function
0	0	Normal Operation
0	1	PIO input with pull-up/pull-down
1	0	PIO output
1	1	PIO input without pull-up/pull-down



**Register Offset:** 7Ah  
**Register Name:** PIO Data 1 Register  
**Reset Value :**

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

PDATA[31:16]

Bit	Name	Attribute	Description
15-0	PDATA [31:16]	R/W	PIO Data Bits. These bits PDATA[31:16] are mapped to the PIO[31:16] that indicate the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

**Register Offset:** 78h  
**Register Name:** PIO Direction 1 Register  
**Reset Value :** FF9Fh

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

PDIR[31:16]

Bit	Name	Attribute	Description
15-0	PDIR [31:16]	R/W	PIO Direction Register. Set 1: Configure the PIO pin as an input pin. Set 0: Configure the PIO pin as an output or as a pin of normal function.

**Register Offset:** 76h  
**Register Name:** PIO Mode 1 Register  
**Reset Value :** 0000h

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

PMODE[(31:16)]

Bit	Name	Attribute	Description
15-0	PMODE [31:16]	R/W	PIO Mode Bit. The definitions of PIO pins are configured by the combination of PIO Mode and PIO Direction. The PIO pins are programmed individually. The definitions (PIO Mode, PIO Direction) for the functions of PIO pins: ( 0 , 0 ) – Normal operation , ( 0 , 1 ) – PIO input with pull-up/pull-down ( 1 , 0 ) – PIO output , ( 1 , 1 ) -- PIO input without pull-up/pull-down

**Register Offset:** 74h  
**Register Name:** PIO Data 0 Register  
**Reset Value :**

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

PDATA[15:0]

Bit	Name	Attribute	Description
15-0	PDATA [15:0]	R/W	PIO Data Bus. These bits PDATA[15:0] are mapped to the PIO[15:0] that indicate the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

**Register Offset:** 72h  
**Register Name:** PIO Direction 0 Register  
**Reset Value :** FC4Fh

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

PDIR[15:0]

Bit	Name	Attribute	Description
15-0	PDIR [15:0]	R/W	PIO Direction Register. Set 1: Configure the PIO pin as an input pin. Set 0: Configure the PIO pin as an output or as a pin of normal function.

**Register Offset:** 70h  
**Register Name:** PIO Mode 0 Register  
**Reset Value :** 0000h

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

PMODE[15:0]

Bit	Name	Attribute	Description
15-0	PMODE [15:0]	R/W	PIO Mode Bus.

## 18. CACHE Controller

### 18.1 Cache Control Register

**Register Offset:** FEC0h  
**Register Name:** Cache Control Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICE	DCE	Reserved	NCR3	NCR2	NCR1	NCR0	WIR	Reserved							

Bit	Name	Attribute	Description
15	ICE	R/W	Instruction Cache enable when set
14	DCE	R/W	Data Cache enable when set
13-12	Rsvd	RO	Reserved
11	NCR3	R/W	Non-Cache region3 enable when set
10	NCR2	R/W	Non-Cache region2 enable when set
9	NCR1	R/W	Non-Cache region1 enable when set
8	NCR0	R/W	Non-Cache region0 enable when set
7	WIR	R/W	Write Invalid region enable when set
6-0	Rsvd	RO	Reserved

### 18.2 Non-Cache Region Register

**Register Offset:** FEC2h  
**Register Name:** Non-Cache Region0 Start Address Low Register  
**Reset Value :** ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRS[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	NCRS	R/W	Non-Cache Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region start address [2:0]

**Register Offset:** FEC4h  
**Register Name:** Non-Cache Region0 Start Address High Register  
**Reset Value :** -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRS[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRS	R/W	Non-Cache Region start address [23:16]

**Register Offset:** FEC6h  
**Register Name:** Non-Cache Region0 End Address Low Register  
**Reset Value :** ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRE[15:3]													reserved		

Bit	Name	Attribute	Description
15-3	NCRE	R/W	Non-Cache Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region end address [2:0]

**Register Offset:** FEC8h  
**Register Name:** Non-Cache Region0 End Address High Register  
**Reset Value :** -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRE[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRE	R/W	Non-Cache Region end address [23:16]

**Register Offset:** FECAh  
**Register Name:** Non-Cache Region1 Start Address Low Register  
**Reset Value :** ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRS[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	NCRS	R/W	Non-Cache Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region start address [2:0]

**Register Offset:** FECCh  
**Register Name:** Non-Cache Region1 Start Address High Register  
**Reset Value :** -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRS[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRS	R/W	Non-Cache Region start address [23:16]

**Register Offset:** FECEh  
**Register Name:** Non-Cache Region1 End Address Low Register  
**Reset Value :** ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRE[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	NCRE	R/W	Non-Cache Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region end address [2:0]

**Register Offset:** FED0h  
**Register Name:** Non-Cache Region1 End Address High Register  
**Reset Value :** -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRE[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRE	R/W	Non-Cache Region end address [23:16]

**Register Offset:** FED2h  
**Register Name:** Non-Cache Region2 Start Address Low Register  
**Reset Value :** ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRS[15:3]												Reserved			

Bit	Name	Attribute	Description
15-3	NCRS	R/W	Non-Cache Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region start address [2:0]

**Register Offset:** FED4h  
**Register Name:** Non-Cache Region2 Start Address High Register  
**Reset Value :** -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRS[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRS	R/W	Non-Cache Region start address [23:16]

**Register Offset:** FED6h  
**Register Name:** Non-Cache Region2 End Address Low Register  
**Reset Value :** ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRE[15:3]												Reserved			

Bit	Name	Attribute	Description
15-3	NCRE	R/W	Non-Cache Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region end address [2:0]

**Register Offset:** FED8h  
**Register Name:** Non-Cache Region2 End Address High Register  
**Reset Value :** ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRE[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRE	R/W	Non-Cache Region end address [23:16]

**Register Offset:** FEDAh  
**Register Name:** Non-Cache Region3 Start Address Low Register  
**Reset Value :** ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRS[15:3]												Reserved			

Bit	Name	Attribute	Description
15-3	NCRS	R/W	Non-Cache Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region start address [2:0]

**Register Offset:** FEDCh  
**Register Name:** Non-Cache Region3 Start Address High Register  
**Reset Value :** -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRS[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRS	R/W	Non-Cache Region start address [23:16]

**Register Offset:** FEDEh  
**Register Name:** Non-Cache Region3 End Address Low Register  
**Reset Value :** ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRE[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	NCRE	R/W	Non-Cache Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region end address [2:0]

**Register Offset:** FEE0h  
**Register Name:** Non-Cache Region3 End Address High Register  
**Reset Value :** -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRE[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRE	R/W	Non-Cache Region end address [23:16]



### 18.3 Write Invalid Region Register

**Register Offset:** FEE2h  
**Register Name:** Write Invalid Region Start Address Low Register  
**Reset Value :** ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WIRS[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	WIRS	R/W	Write Invalid Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Write Invalid Region start address [2:0]

**Register Offset:** FEE4h  
**Register Name:** Write Invalid Region Start Address High Register  
**Reset Value :** -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								WIRS[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	WIRS	R/W	Write Invalid Region start address [23:16]

**Register Offset:** FEE6h  
**Register Name:** Write Invalid Region End Address Low Register  
**Reset Value :** ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WIRE[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	WIRE	R/W	Write Invalid Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Write Invalid Region start address [2:0]

Register Offset: FEE8h  
Register Name: Write Invalid Region End Address High Register  
Reset Value : -----

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Reserved	WIRE[23:16]
----------	-------------

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	WIRE	R/W	Write Invalid Region end address [23:16]

← - - 格式化: 項目符號及編號

## 19. SDRAM Controller

### 19.1 SDRAM Mode Set Register

**Register Offset:** F2h  
**Register Name:** SDRAM Mode Set Register  
**Reset Value :** 0020h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								0	LAT[2:0]		0	BL[2:0]			

Bit	Name	Attribute	Description																
15-7	Rsvd	RO	Reserved																
6-4	LAT[2:0]	R/W	CAS_n Latency Select. Refer to the following list: <table><thead><tr><th><u>LAT [2:0]</u></th><th><u>CAS_n Latency</u></th></tr></thead><tbody><tr><td>0 0 0</td><td>Reserved</td></tr><tr><td>0 0 1</td><td>Reserved</td></tr><tr><td>0 1 0</td><td>2 (Default)</td></tr><tr><td>0 1 1</td><td>3</td></tr><tr><td>1 0 0</td><td>Reserved</td></tr><tr><td>1 0 1</td><td>Reserved</td></tr><tr><td>1 1 0</td><td>Reserved</td></tr></tbody></table>	<u>LAT [2:0]</u>	<u>CAS_n Latency</u>	0 0 0	Reserved	0 0 1	Reserved	0 1 0	2 (Default)	0 1 1	3	1 0 0	Reserved	1 0 1	Reserved	1 1 0	Reserved
<u>LAT [2:0]</u>	<u>CAS_n Latency</u>																		
0 0 0	Reserved																		
0 0 1	Reserved																		
0 1 0	2 (Default)																		
0 1 1	3																		
1 0 0	Reserved																		
1 0 1	Reserved																		
1 1 0	Reserved																		
3	Rsvd	RO	1'b0.																
2-0	BL[2:0]	<del>RO</del>	Burst Length																

刪除: R/W

刪除: Select

刪除: Set to 3'b000 for single read/write only. (Default is 000b)

格式化: 項目符號及編號

### 19.2 SDRAM Control Register

**Register Offset:** F4h  
**Register Name:** SDRAM Control Register  
**Reset Value :** 0001h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										SSSEL1	SSSEL0	SREF	Rsvd	SDRAM EN	

Bit	Name	Attribute	Description								
15-5	Rsvd	RO	Reserved								
4-3	SSSEL[1:0]	R/W	<div>The SDRAM Size Select bit. (Default is 2'b0)</div> <table><tr><th>SSEL1-0</th><th>SDRAM Size Select</th></tr><tr><td>0 0</td><td>1Mx16 bits</td></tr><tr><td>0 1</td><td>4Mx16 bits</td></tr><tr><td>1 0</td><td>Reserved</td></tr></table>	SSEL1-0	SDRAM Size Select	0 0	1Mx16 bits	0 1	4Mx16 bits	1 0	Reserved
SSEL1-0	SDRAM Size Select										
0 0	1Mx16 bits										
0 1	4Mx16 bits										
1 0	Reserved										

			1 1 ----- Reserved
2	SREF	R/W	Self-Refresh Enable. Set 1: Enable Self-Refreshed when SDRAM is in power mode. Set 0: Disable Self-Refreshed. (Default)
1	Rsvd	RO	Reserved
0	SDRAMEN	R/W	SDRAM Enable. Set 1: Enable SDRAM. (Default) Set 0: Disable SDRAM.

### 19.3 SDRAM Timing Parameter Register

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Register Offset: F6h  
Register Name: SDRAM Timing Parameter Register  
Reset Value : F933h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SREXT[2:0]			TWR	MRC[3:0]			MPR[3:0]			RCD[3:0]					

刪除: 3

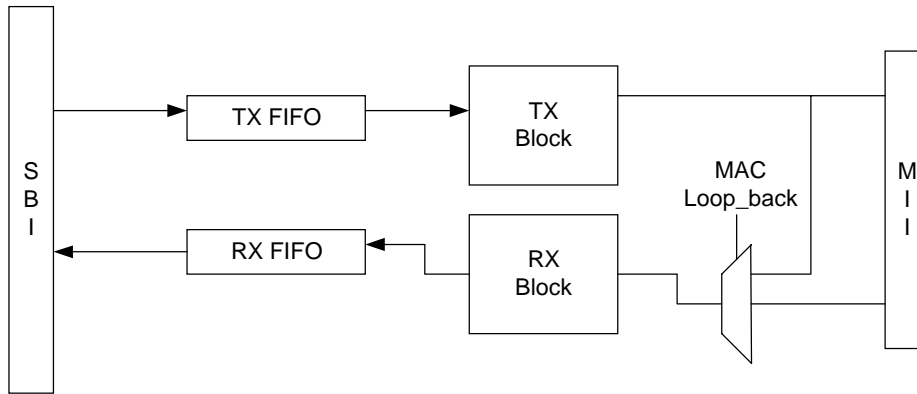
Bit	Name	Attribute	Description
15-13	SREXT[2:0]	R/W	Self-Refresh Exit Time ( $t_{SREX}$ ). The Self-Refresh Exit Time can be programmed from 0 to 15 Clocks.
12	TWR	R/W	Write Recovery Time. 1: 1 Clock cycle. 0: 2 Clocks cycle.
11-8	MRC[3:0]	R/W	Min Row Cycle Time ( $t_{RC}$ ). It can be programmed from 0 to 15 Clocks.
7-4	MPR[3:0]	R/W	Min Pre-charge Time ( $t_{RP}$ ). It can be programmed from 0 to 15 Clocks.
3-0	RCD[3:0]	R/W	Row to Column Delay time ( $t_{RCD}$ ). It can be programmed from 0 to 15 Clocks.

刪除: 2

刪除: 3

格式化: 項目符號及編號

## 20. Fast Ethernet Controller



SBI : System Bus Interface  
MAC Block Diagram

### 20.1 RX Descriptor Format

格式化: 項目符號及編號

15	3	2	1	0
DRST				
DRLEN				
DRBP				0 0
				DRBP [23:16]
DRNX				0 0
				DRNX [23:16]
				HIDX[5:0]
Reserve2				
Reserve3				

#### 1. DRST

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
O	RXOK	Reserved	PHY ERR	DRI BBLE	OBL	LONG	RUNT	CRC ERR	BROAD CAST	MULTI CAST	MCH	MIDH	MID		

The RX circuit will stop receiving packet if Owner Bit=0.

DRST [14:0]: RX Status. The MAC will update the RX status field after frame receiving is complete.

Bit	Name	Description
15	O	Owner Bit. Set1: MAC. Set0: CPU.

14	RXOK	RX successful. This bit indicates that the packet was received successfully without error. It includes: (1) RX_ER = 0 (MII interface). (2) Ignore DRIBBLE status. (3) No over buffer length. (4) Without CRC error. (5) Not a LONG packet. (6) Not a RUNT packet. (7) No FIFO Full.
13-12	Rsvd	Reserved.
11	PHYERR	PHY RX Error packet. Read 1 means that an error occurred in receiving packets on MII interface.
10	DRIBBLE	Dribble packet. Read 1 means the received packet is a dribble packet.
9	OBL	Over Buffer Length. Read 1 means the received packet length > buffer maximum length.
8	LONG	Long packet. Read 1 means the received packet length > maximum packet length.
7	RUNT	Runt packet. Read 1 means the received packet length < 64 Bytes.
6	CRCERR	CRC Error packet. Read 1 means receiving a packet with CRC errors.
5	BROADCAST	It indicates that the received packet is a broadcast packet.
4	MULTICAST	It indicates that the received packet is a multicast packet.
3	MCH	Multicast Hit. It indicates that the received packet hits one of the hash-table bits.
2	MIDH	MID table is hit.
1-0	MID	Index of matched MIDx. These two bits indicate that the received packet hits one of the MID groups.

## 2. DRLEN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						DRLEN									

Bit	Name	Description
15-11	Rsvd	Reserved.
10-0	DRLEN	The size of the received frame.

## 3. DRBP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DRBP																							

Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DRBP	RX Data Buffer Pointer. This is a 24-bit address pointer and DRBP [1:0] is always 2'b00.

#### 4. DRNX

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Reserved	DRNX
----------	------

Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DRNX	RX Next Frame Descriptor Pointer. This is a 24-bit descriptor address pointer and DRNX [1:0] is always 2'b00. This field must be pointed to next descriptor start address or its start address.

#### 5. HIDX

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Reserved	HIDX
----------	------

Bit	Name	Description
15-6	Rsvd	Reserved.
5-0	HIDX	HIDX[5:0] is a hash index. If MCR1[14] is set to 1, the hash index number will be written into RX description.

#### 6. Reserve2

#### 7. Reserve3

#### Note:

1. RX Descriptor start address and Data Buffer start address must be Double-Word alignment.
2. The RX packet will be filtered out if its length is less than 6. (Not complete DA information.)

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## 20.2 TX Descriptor Format

15				3	2	1	0
DTST							
DTLEN							
DTBP						0	0
						DTBP [23:16]	
DTNP						0	0
						DTNP [23:16]	

### 1. DTST

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
O	TXOK	DIS CRC	Reserved					TXFUR	LATEC	EXCEE DC	COLCNT				

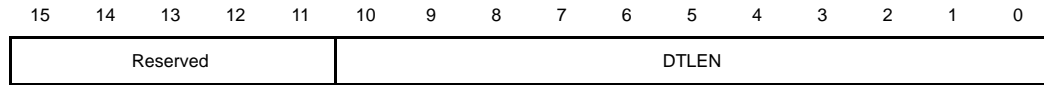
The TX circuit will stop transmitting packet if the Owner Bit=0

DTST [14:0]: TX Status and packet control. The MAC will update the TX status field after frame transmission is completed. The control bit is for each packet usage.

Bit	Name	Description
15	O	Owner Bit. Set1: MAC. Set0: CPU.
14	TXOK	TX packet successful. This bit indicates that the packet was transmitted successfully without error. It includes: (1) No late collision. (2) No excessive collision. (3) No TX FIFO under-run. (4) No lost carrier.
13	DISCRC	Disable append CRC field. This is a control bit. =1: disable CRC append. =0: enable CRC append on TX packet. When the status is updated, this bit will keep in previous setting.
12-7	Rsvd	Reserved
6	TXFUR	FIFO Under-Run.
5	LATEC	Late Collision.
4	EXCEEDC	Exceed Collision.
3-0	COLCNT	Collision Counts.

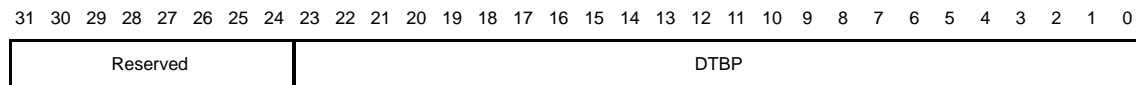


## 2. DTLEN



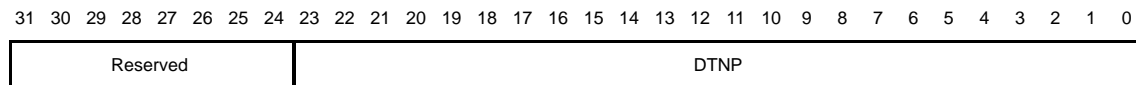
Bit	Name	Description
15-11	Rsvd	Reserved.
10-0	DTLEN	The length of the transmitted packet.

## 3. DTBP



Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DTBP	TX Buffer Pointer. This is a 24-bit address pointer.

## 4. DTNP



Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DTNP	TX Next Descriptor Pointer. This is a 24-bit descriptor address pointer and DTNP [1:0] is always 2'b00. This field must be pointed to next descriptor start address or its start address.

### Note:

- TX Descriptor start address must be Double-Word alignment.
- TX Data Buffer start address can be any byte alignment address.
- Driver needs to take care that the transmitted data are less than 60 bytes.

刪除:

刪除: and TX Data Buffer  
start address

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### 20.3 MCR0: MAC Control Register 0 (00h)

**Register Offset:** 00h  
**Register Name:** MCR0: MAC Control Register 0  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FULLD	TXEIE	Rsvd	XMTEN	Reserved	FCEN	AMCP	RXEIE	FBCP	PROM	ADRB	ALONG	ARUNT	ACRCER	RCVEN	

Bit	Name	Attribute	Description
15	FULLD	R/W	Full Duplex. Set 1: Full duplex. Set 0: Half duplex. (Default)
14	TXEIE	R/W	TX Early Interrupts Enable. Set 1: MAC will generate one TX early interrupt when the data are transmitted over early interrupt threshold (see MCR1 [7:6]). Set 0: TX early interrupt will be disabled.
13	Rsvd	RO	Reserved
12	XMTEN	R/W	Transmission Enable
11-10	Rsvd	RO	Reserved
9	FCEN	R/W	Flow Control Function Enable. Set 1: will enable flow control. Set 0: will disable flow control.
8	AMCP	R/W	Accept Multicast Packet. Set 1: will enable hash table function. Set 0: will disable hash table function.
7	RXEIE	R/W	RX Early Interrupts Enable. Set to 1, MAC will generate one RX early interrupt when the data are received over early interrupt threshold (see MCR1 [7:6]). Set 0: RX early interrupt will be disabled.
6	FBCP	R/W	Filter Broadcast Packet. Set 1: to filter broadcast packet. Set 0: to accept broadcast packet.
5	PROM	R/W	Promiscuous Mode. Set 1: MAC will receive all packets without checking the MAC address. Set 0: MAC will only receive the packet that hits the MAC address.
4	ADRB	R/W	Accept DRIBBLE packet. Set 1: Enable to accept dribble packets. Set 0: Disable.
3	ALONG	R/W	Accept Long packet. Set 1: Enable to accept long packets. Set 0: Disable.
2	ARUNT	R/W	Accept RUNT packet. Set 1: Enable to accept runt packets. The packets which length > 6 and < 64 will be accepted, but the packets which length >0 and < 6 will be rejected. Set 0: Disable to accept runt packets.
1	ACRCER	R/W	Accept CRC Error packet. Set 1: Enable. Set 0: Disable.

0	RCVEN	R/W	Receive Enable. Set 1: Enable to receive packets. Set 0: Disable packet receive.
---	-------	-----	--

## 20.4 MCR1: MAC Control Register 1 (04h)

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**Register Offset:** 04h  
**Register Name:** MCR1: MAC Control Register 1  
**Reset Value :** 0010h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUCP	WIDX	Reserved	TPF	ECR	EITH [1:0]	MAXLEN [1:0]	0	0	LBM	MRST					

Bit	Name	Attribute	Description
15	AUCP	R/W	Filter uni-cast packet by hash-table. Set 1: Enable. Set 0: Disable.
14	WIDX	R/W	Write the hash index number that was hit by hash-table. Set 1: Enable to write the WIDX [5:0] into Rx descriptor. Set 0: Disable this function.
13-10	Rsvd	RO	Reserved
9	TPF	RO	Trigger Pause Frame to be transmitted. If flow control (FCEN bit in MCR0 [9]) is enabled, this bit will be set automatically when received descriptor unavailable happens. TPF refers to XMTEN bit (MCR0 [12]). When XMTEN bit is set, the pause frame can be sent.
8	ECR	R/W	Excessive Collision Retransmit times. 0: 16 times. (Default) 1: 32 times.
7-6	EITH [1:0]	R/W	Early Interrupt Threshold. 00: 1129 bytes. (Default) 01: 1257 bytes. 10: 1385 bytes. 11: 1513 bytes.
5-4	MAXLEN [1:0]	R/W	Maximum Packet Length Selector. Define the length of long packets. 01: 1518 bytes. (Default) 10: 1522 bytes. 11: 1534 bytes. 00: 1537 bytes.
3-2	Rsvd	R/O	Reserved
1	LBM	R/W	Loop-Back mode. 0: Normal Mode. (Default) 1: MAC Loop-Back.
0	MRST	R/W	MAC Reset. Set 1 to reset MAC. After reset, this bit will be cleared to 0.

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## 20.5 MBCR: MAC Bus Control Register (08h)

**Register Offset:** 08h  
**Register Name:** MBCR: MAC Bus Control Register  
**Reset Value :** 1F1Ah

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			RHPT [4:0]					Reserved		RXFTH [1:0]		TXFTH [1:0]		FIFOTL [1:0]	

**PS. Update this register only when RCVEN=0**

Bit	Name	Attribute	Description
15-13	Rsvd	RO	Reserved
12-8	RHPT [4:0]	R/W	SDRAM Bus Request High Priority Timer. When MAC issues a bus request to SDRAM arbiter, this timer will start to count down. After this timer is timeout, if SDRAM arbiter is still not granted to MAC, the SDRAM bus request will become high priority. Wait time = 0 ~15 host clocks. (Default=15 host clocks)
7-6	Rsvd	RO	Reserved
5-4	RXFTH [1:0]	R/W	RX FIFO Data Threshold. MAC receive machine starts to move the received data into host memory when receiving data over the RX FIFO threshold. 00: 8 bytes. 01: 16 bytes. (Default) 10: 32 bytes. 11: 64 bytes.
3-2	TXFTH [1:0]	R/W	TX FIFO Data Threshold. MAC transmit machine starts to send out packets to PHY when transmitting data into TX FIFO over the threshold. 00: 16 bytes. 01: 32 bytes. 10: 64 bytes. (Default) 11: 96 bytes.
1-0	FIFOTL [1:0]	R/W	FIFO Transfer Length. The every transfer data length between MAC FIFO and SDRAM. 00: 4 bytes. 01: 8 bytes. 10: 16 bytes. (Default) 11: 32 bytes.

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## 20.6 MTICR: TX Interrupt Control Register (0Ch)

**Register Offset:** 0Ch  
**Register Name:** MTICR: TX Interrupt Control Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TXINTC [3:0]				Reserved		TXTIMER [5:0]					

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved
11-8	TXINTC [3:0]	R/W	TX Interrupt Control. 0: Turn off this function. N: Generate an interrupt after sending N packets (1~15 packets).
7-6	Rsvd	RO	Reserved
5-0	TXTIMER [5:0]	R/W	Wait TX Timer. When timeout, it automatically generates an interrupt. Timer waiting time: $(63 + \text{TXTIMER} * 64)$ TX clock

## 20.7 MRICR: RX Interrupt Control Register (10h)

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**Register Offset:** 10h  
**Register Name:** MRICR: RX Interrupt Control Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				RXINTC [3:0]				Reserved		RXTIMER [5:0]					

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved
11-8	RXINTC [3:0]	R/W	RX Interrupt Control. 0: Turn off this function. N: Generate an interrupt after N packets (1~15 packets) are received.
7-6	Rsvd	RO	Reserved
5-0	RXTIMER [5:0]	R/W	Wait RX Timer. When timeout, it automatically generates an interrupt. Timer waiting time: $(63 + \text{RXTIMER} * 64)$ RX clock

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## 20.8 MTPR: TX Poll Command Register (14h)

**Register Offset:** 14h  
**Register Name:** MTPR: TX Poll Command Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														TM2TX	

Bit	Name	Attribute	Description
15-1	Rsvd	RO	Reserved
0	TM2TX	R/W	Trigger MAC to Transmit. When Write: Trigger MAC to check TX description owner bit. If owner bit=0, MAC will standby until the owner bit=1 to start transmission. When Read: TM2TX is current transmission status. When TM2TX= 1, it means MAC is in transmitting. When TM2TX= 0, it means transmission was completed.

## 20.9 MRBSR: RX Buffer Size Register (18h)

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**Register Offset:** 18h  
**Register Name:** MRBSR: RX Buffer Size Register  
**Reset Value :** 0600h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					RBSZ [10:0]										RBSZ[1:0]

**PS. Update this register only when RCVEN=0**

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
10-2	RBSZ [10:2]	R/W	RX Buffer Size Bit10~Bit2 for all RX <a href="#">frame data buffer of</a> Descriptors.
1-0	RBSZ [1:0]	R/W	RX Buffer Size Bit1:0 must be 00.

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## 20.10 MRDCR: RX Descriptor Control Register (1Ah)

**Register Offset:** 1Ah  
**Register Name:** MRDCR: RX Descriptor Control Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXPT [7:0]								RXDESPAN [7:0]							

Bit	Name	Attribute	Description
15-8	RXPT [7:0]	R/W	RX Descriptor Threshold value. MAC controller will send TX Pause Frame when available RX Descriptor reaches this threshold value.
7-0	RXDESPAN [7:0]	R/W	RX Descriptor Available Number for flow-control. When MAC finishes one descriptor data transfer into RX buffer, the RX descriptor available number will decrease 1 automatically. Use "IN" instruction to read this register and "OUT" instruction to increase the register value. When RCVEN=0, use "OUT" instruction to setup RX descriptor available number. When RCVEN=1, use "OUT" instruction to increase RX descriptor available number. This register must be initialized before RCVEN = 1.

## 20.11 MLSR: MAC Last Status Register(1Ch)

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**Register Offset:** 1Ch  
**Register Name:** MLSR: MAC Last Status Register  
**Reset Value :** 0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXFOR	LATEC	EXCEED C	Rsvd	PHYSTS	RXDESP UA	TXFUR	Rsvd	PHYEER	DRIBBLE	OBL	LONG	RUNT	CRCERR	BROAD CAST	MULTI CAST

**PS. The MAC last time status. It is updated by next packet coming.**

Bit	Name	Attribute	Description
15	R <del>X</del> FOR	RO	RX FIFO Over-Run
14	LATEC	RO	Transmit Late Collision.
13	EXCEEDC	RO	Transmit Exceed Collision.
12	Rsvd	RO	Reserved
11	PHYSTS	RO	The value is the <u>status of</u> input pin PHY_CHG.

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10	RXDESPUA	RO	RX Descriptor Unavailable.
9	TXFUR	RO	TX FIFO Under-Run.
8	Rsvd	RO	Reserved
7	PHYERR	RO	PHY RX Error.
6	DRIBBLE	RO	Dribble Packet.
5	OBL	RO	Received Packet Length Over Buffer Length.
4	LONG	RO	Received Packets Too Long.
3	RUNT	RO	Received Packets Too Short.
2	CRCERR	RO	Received Packets CRC Error.
1	BROADCAST	RO	Received Broadcast Packets.
0	MULTICAST	RO	Received Multicast Packets.

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## 20.12 MMDIO: MDIO Control Register (20h)

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**Register Offset:** 20h  
**Register Name:** MMDIO: MDIO Control Register  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd		MIWR	MIIRD	PHYAD [4:0]				Reserved			REGAD [4:0]				

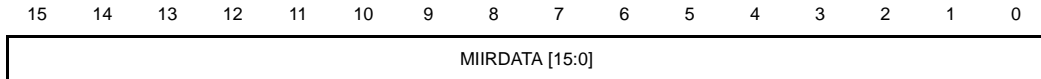
Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14	MIIWR	R/W	MDIO Write. Set 1 to write MIIWDATA [15:0] to MDIO. It will be cleared after the operation is completed.
13	MIIRD	R/W	MDIO Read. Set 1 to read data from MDIO into MIIRDATA [15:0]. It will be cleared after the operation is completed.
12-8	PHYAD [4:0]	R/W	PHY address.
7-5	Rsvd	RO	Reserved
4-0	REGAD [4:0]	R/W	REG address.

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### 20.13 MMRD: MDIO Read Data Register (24h)

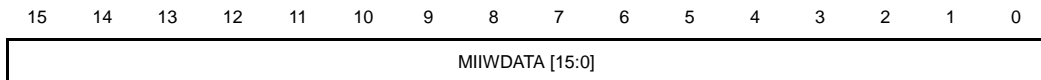
**Register Offset:** 24h  
**Register Name:** MMRD: MDIO Read Data Register  
**Reset Value :** 0000h



Bit	Name	Attribute	Description
15-0	MIIRDATA [15:0]	RO	MII Read Data. The data, read from MDIO, are put in this register.

### 20.14 MMWD: MDIO Write Data Register (28h)

**Register Offset:** 28h  
**Register Name:** MMRD: MDIO Write Data Register  
**Reset Value :** 0000h



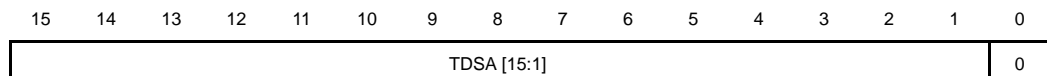
Bit	Name	Attribute	Description
15-0	MIIWDATA [15:0]	R/W	MII Write Data. The data, intended for being written to MDIO, are put in this register.

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## 20.15 MTDSA0: TX Descriptor Start Address 0 (2Ch)

Register Offset: 2Ch  
Register Name: MTDSA0: TX Descriptor Start Address 0  
Reset Value : 0000h



**PS. Initial this register only when XMTEN=0**

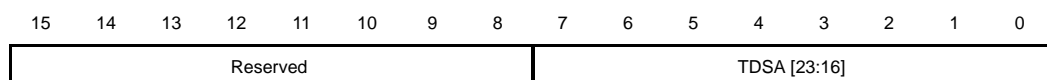
Bit	Name	Attribute	Description
15-1	TDSA [15:1]	R/W	TX Descriptor Start Address Bit 15 - Bit 1 that are currently being sent.
0	0	RO	This bit must be 0.

**Note:** The first TX descriptor start address TDSA [23:0] = {MTDSA1 [7:0], MTDSA0 [15:0]} must be Double-Word alignment. MAC will update the TX descriptor start address when the previous TX has been finished.

刪除: and the start address

## 20.16 MTDSA1: TX Descriptor Start Address 1 (30h)

Register Offset: 30h  
Register Name: MTDSA1: TX Descriptor Start Address 1  
Reset Value :



**PS. Initial this register only when XMTEN=0**

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-0	TDSA [23:16]	RW	TX Descriptor Start Address Bit 23-16 that are currently being sent.

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### 20.17 MRDSA0: RX Descriptor Start Address 0 (34h)

**Register Offset:** 34h  
**Register Name:** MRDSA0: RX Descriptor Start Address 0  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDSA [15:1]															0

**PS. Initial this register only when RCVEN=0**

Bit	Name	Attribute	Description
15-1	RDSA [15:1]	R/W	RX Descriptor Start Address Bit 15-1.
0	0	RO	This bit must be 0.

**Note:** The first RX descriptor start address RDSA [23:0] = {MRDSA1 [7:0], MRDSA0 [15:0]} must be Double-Word alignment. MAC will update the RX descriptor start address after the previous RX has been finished.

刪除: and the start address

### 20.18 MRDSA1: RX Descriptor Start Address 1 (38h)

**Register Offset:** 38h  
**Register Name:** MRDSA1: RX Descriptor Start Address 1  
**Reset Value :**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								RDSA [23:16]							

**PS. Initial this register only when RCVEN=0**

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-0	RDSA [23:16]	RW	The first RX Descriptor Start Address Bit 23-16.

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## 20.19 MISR: INT Status Register (3Ch)

**Register Offset:** 3Ch  
**Register Name:** MISR: INT Status Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						PCHG	ECNTO	TXEI	Reserved		TXEND	RXEI	RXFF	RXDUA	RXEND

Bit	Name	Attribute	Description
15-10	Rsvd	RO	Reserved.
9	PCHG	RC	PHY Media Changed Interrupt status.
8	ECNTO	RC	Event Counter Overflow Interrupt status.
7	TXEI	RC	TX Early Interrupt status.
6-5	Rsvd	RO	Reserved.
4	TXEND	RC	This bit indicates Transmit Packet Finish Interrupt status.
3	RXEI	RC	RX Early Interrupt status.
2	RXFF	RC	RX FIFO Full Interrupt status.
1	RXDUA	RC	This bit indicates RX Descriptor Unavailable Interrupt status.
0	RXEND	RC	This bit indicates Receive Packet Finish Interrupt status.

**Note:** RC = Read Clear

## 20.20 MIER: INT Enable Register (40h)

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**Register Offset:** 40h  
**Register Name:** MIER: INT Enable Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						MCHGE	ECNTO E	TXEIEN	Reserved		TXENDE	RXEIE	RXFFE	RXDNA E	RXEND E

Bit	Name	Attribute	Description
15-10	Rsvd	RO	Reserved.
9	MCHGE	RW	PHY Link Changed Interrupt Enable Set 1: Enable MAC to generate interrupts to CPU.
8	ECNTOE	R/W	Event Counter Overflow Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
7	TXEIEN	R/W	TX Early Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.

6-5	Rsvd	RO	Reserved.
4	TXENDE	R/W	Transmit Packet Finish Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
3	RXEIE	R/W	RX Early Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
2	RXFFE	R/W	RX FIFO Full Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
1	RXDNAE	R/W	RX Descriptor Unavailable Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
0	RXENDE	R/W	Receive Packet Finish Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.

## 20.21 MECISR: Event Counter INT Status Register(44h)

格式化: 項目符號及編號

**Register Offset:** 44h  
**Register Name:** MECISR: Event Counter INT Status Register  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TDPCI	LCCI	STPCI	RFFCI	RDUCI	Rsvd	LONGCI	RUNTCI	CRCECI	BCCI	MCCI	SRPCI

The correspond bit in Event Counter INT status register will be set when the MSB bit in related Event Counter register is set to 1. Reading the Event Counter register will clear the corresponding bits. Those event counters will keep increasing until reaching 255 or 65535.

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved.
11	TDPCI	RO	TX FIFO under-run Dropped Packet Counter Interrupt status.
10	LCCI	RO	TX Late Collision Counter Interrupt status.
9	STPCI	RO	TX Successfully <u>package counter</u> Interrupt status.
8	RFFCI	RO	RX FIFO Full Counter Interrupt status.
7	RDUCI	RO	RX Descriptor Unavailable Dropped Packet Counter Interrupt status.
6	Rsvd	RO	Reserved.
5	LONGCI	RO	RX Long Packet Counter Interrupt status.
4	RUNTCI	RO	RX Runt Packet Counter Interrupt status.
3	CRCECI	RO	RX CRC Error Packet Counter Interrupt status.
2	BCCI	RO	RX Broadcast Packet Counter Interrupt status.
1	MCCI	RO	RX Multicast Packet Counter Interrupt status.
0	SRPCI	RO	RX Successfully Packet Counter Interrupt status.

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## 20.22 MECIER: Event Counter INT Enable Register (48h)

Register Offset: 48h  
Register Name: MECIER: Event Counter INT Status Register  
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TDPCIE	LCCIE	STPCIE	RFFCIE	RDUCIE	Rsvd	LONGCIE	RUNTCIE	CRCECIE	BCCIE	MCCIE	SRPCIE

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved.
11	TDPCIE	RW	TX FIFO under-run Dropped Packet Counter Interrupt Enable
10	LCCIE	R/W	TX Late Collision Counter Interrupt Enable.
9	STPCIE	R/W	TX Successfully Packet Counter Interrupt Enable.
8	RFFCIE	R/W	RX FIFO Full Counter Interrupt Enable.
7	RDUCIE	R/W	RX Descriptor Unavailable Dropped Packet Counter Interrupt Enable.
6	Rsvd	RO	Reserved.
5	LONGCIE	R/W	RX Long Packet Counter Interrupt Enable.
4	RUNTCIE	R/W	RX Runt Packet Counter Interrupt Enable.
3	CRCECIE	R/W	RX CRC Error Packet Counter Interrupt Enable.
2	BCCIE	R/W	RX Broadcast Packet Counter Interrupt Enable.
1	MCCIE	R/W	RX Multicast Packet Counter Interrupt Enable.
0	SRPCIE	R/W	RX Successfully Packet Counter Interrupt Enable.

**Note:** Reading any one of all the following event counter registers will clear its value to 0.

## 20.23 MRCNT: Successfully Received Packet Counter (50h)

Register Offset: 50h  
Register Name: MRCNT: Successfully Received Packet Counter  
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRPCNT [15:0]															

Bit	Name	Attribute	Description
15-0	SRPCNT [15:0]	RC	Successfully Received Packet Counter

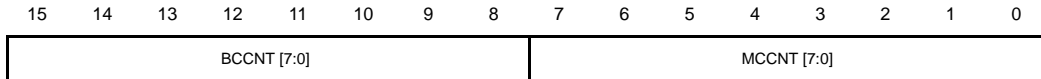
**Note:** RC = Read Clear

← 格式化: 項目符號及編號

← 格式化: 項目符號及編號

## 20.24 MECNT0: Event Counter 0 (52H)

**Register Offset:** 52h  
**Register Name:** MECNT0: Event Counter 0  
**Reset Value :** 0000h

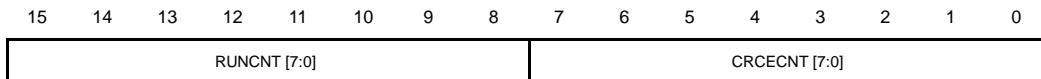


Bit	Name	Attribute	Description
15-8	BCCNT [7:0]	RC	Receive Broadcast Packet Counter.
7-0	MCCNT [7:0]	RC	Receive Multicast Packet Counter.

**Note:** RC = Read Clear

## 20.25 MECNT1: Event Counter 1 (54h)

**Register Offset:** 54h  
**Register Name:** MECNT1: Event Counter 1  
**Reset Value :** 0000h



Bit	Name	Attribute	Description
15-8	RUNCNT [7:0]	RC	Receive Run Packet Counter.
7-0	CRCECNT [7:0]	RC	Receive CRC Error Packet Counter.

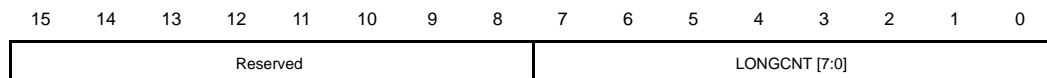
**Note:** RC = Read Clear

格式化: 項目符號及編號

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## 20.26 MECNT2: Event Counter 2 (56h)

**Register Offset:** 56h  
**Register Name:** MECNT2: Event Counter 2  
**Reset Value :** 0000h



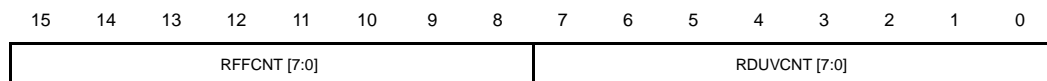
Bit	Name	Attribute	Description
15-8	Rsvd	RC	Reserved
7-0	LONGCNT [7:0]	RC	Receive Long Packet Counter.

**Note:** RC = Read Clear

## 20.27 MCENT3: Event Counter 3 (58h)

← - - 格式化: 項目符號及編號

**Register Offset:** 58h  
**Register Name:** MECNT3: Event Counter 3  
**Reset Value :** 0000h



Bit	Name	Attribute	Description
15-8	RFFCNT [7:0]	RC	RX FIFO Full Packet Counter.
7-0	RDUVCNT [7:0]	RC	RX Descriptor Unavailable Packet lost Counter.

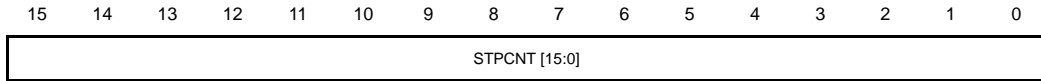
**Note:** RC = Read Clear

← - - 格式化: 項目符號及編號



### 20.28 MTCNT: Successfully Transmit Packet Counter (5Ah)

**Register Offset:** 5Ah  
**Register Name:** MTCNT: Successfully Transmit Packet Counter  
**Reset Value :** 0000h

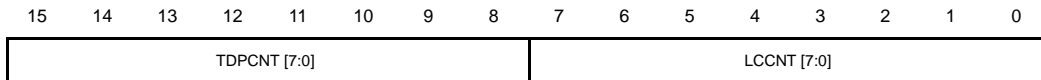


Bit	Name	Attribute	Description
15-0	STPCNT [15:0]	RC	Successfully Transmitted Packet Counter.

**Note:** RC = Read Clear

### 20.29 MCENT4: Event Counter 4 (5Ch)

**Register Offset:** 5Ch  
**Register Name:** MECNT4: Event Counter 4  
**Reset Value :** 0000h

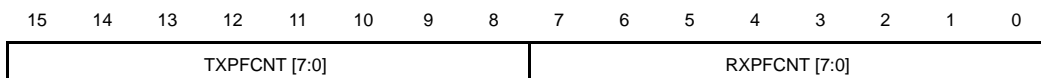


Bit	Name	Attribute	Description
15-8	TDPCNT [7:0]	RC	TX Dropped Packet Counter by TX FIFO under-run.
7-0	LCCNT [7:0]	RC	TX Late Collision Packet Counter.

**Note:** RC = Read Clear

### 20.30 MPCNT: Pause Frame Counter (5Eh)

**Register Offset:** 5Eh  
**Register Name:** MPCNT: Pause Frame Counter  
**Reset Value :** 0000h



Bit	Name	Attribute	Description
15-8	TXPFCNT [7:0]	RC	Transmitted Pause Frame Counter.
7-0	RXPFCNT [7:0]	RC	Received Pause Frame Counter.

**Note:** RC = Read Only

### 20.31 MAR0 ~3: Hash Table Word 0 ~3 (60h, 62h, 64h, 66h)

← 格式化: 項目符號及編號

**Register Offset:** 60h  
**Register Name:** MAR0: Hash Table Word 0  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR0 [15:0]															

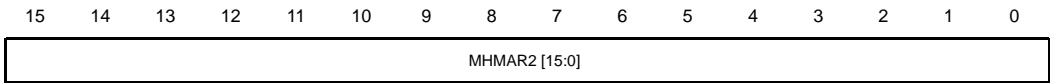
Bit	Name	Attribute	Description
15-0	MHMAR0 [15:0]	R/W	Hash Table Word 0.

**Register Offset:** 62h  
**Register Name:** MAR1: Hash Table Word 1  
**Reset Value :** 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR1 [15:0]															

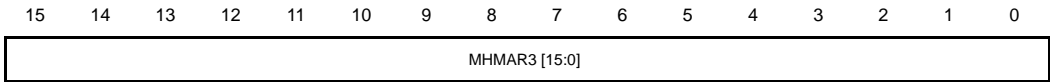
Bit	Name	Attribute	Description
15-0	MHMAR1 [15:0]	R/W	Hash Table Word 1.

**Register Offset:** 64h  
**Register Name:** MAR2: Hash Table Word 2  
**Reset Value :** 0000h



Bit	Name	Attribute	Description
15-0	MHMAR2 [15:0]	R/W	Hash Table Word 2.

**Register Offset:** 66h  
**Register Name:** MAR3: Hash Table Word 3  
**Reset Value :** 0000h



Bit	Name	Attribute	Description
15-0	MHMAR3 [15:0]	R/W	Hash Table Word 3.

20.32

MID0 (68h, 6Ah, 6Ch)

Register Offset:

68h

Register Name:

MID0

Reset Value

:

0000h

15

14

13

12

11

10

9

8

7

6

5

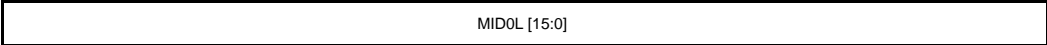
4

3

2

1

0



Register Offset:

6Ah

Register Name:

MID0

Reset Value

:

15

14

13

12

11

10

9

8

7

6

5

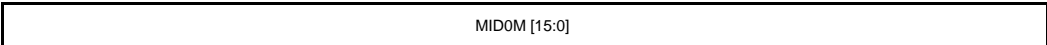
4

3

2

1

0



Register Offset:

6Ch

Register Name:

MID0

Reset Value

:

0000h

15

14

13

12

11

10

9

8

7

6

5

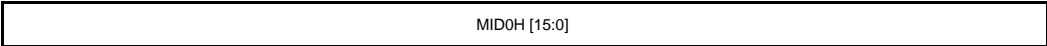
4

3

2

1

0



The MAC/Multicast address MID0 [47:0] = {MID0H [15:0], MID0M [15:0], MID0L [15:0]};

For example: MAC address is 01:02:03:04:05:06, the contents for MID are:

MID0L [15:0] = 0201h

MID0M [15:0] = 0403h

MID0H [15:0] = 0605h

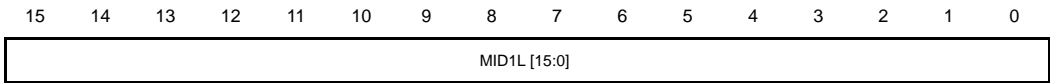
**Bit 15-0: MID0L [15:0]**, the two bytes in the first line of the MAC/Multicast address.

**Bit 15-0: MID0M [15:0]**, the two bytes in the second line of the MAC/Multicast address.

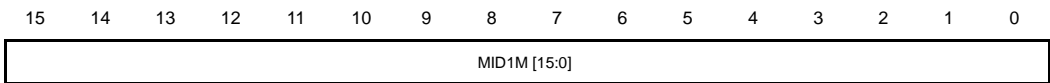
**Bit 15-0: MID0H [15:0]**, the two bytes in the last line of the MAC/Multicast address.

20.33 MID1 (70h, 72h, 74h)

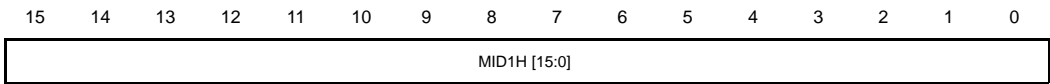
Register Offset: 70h  
Register Name: MID1  
Reset Value : 0000h



Register Offset: 72h  
Register Name: MID1  
Reset Value : 0000h



Register Offset: 74h  
Register Name: MID1  
Reset Value : 0000h



The MAC/Multicast address MID1 [47:0] = {MID1H [15:0], MID1M [15:0], MID1L [15:0]};

Bit 15-0: MID1L [15:0], the two bytes in the first line of the MAC/Multicast address.

Bit 15-0: MID1M [15:0], the two bytes in the second line of the MAC/Multicast address.

Bit 15-0: MID1H [15:0], the two bytes in the last line of the MAC/Multicast address.

20.34 MID2 (78h, 7Ah, 7Ch)

Register Offset: 78h  
Register Name: MID2  
Reset Value : 0000h

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

MID2L [15:0]

Register Offset: 7Ah  
Register Name: MID2  
Reset Value : 0000h

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

MID2M [15:0]

Register Offset: 7Ch  
Register Name: MID2  
Reset Value : 0000h

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

MID2H [15:0]

The MAC/Multicast address MID2 [47:0] = {MID2H [15:0], MID2M [15:0], MID2L [15:0]};

Bit 15-0: MID2L [15:0], the two bytes in the first line of the MAC/Multicast address.

Bit 15-0: MID2M [15:0], the two bytes in the second line of the MAC/Multicast address.

Bit 15-0: MID2H [15:0], the two bytes in the last line of the MAC/Multicast address.

**20.35 MID3 (80h, 82h, 84h)**

**Register Offset:** 80h  
**Register Name:** MID3  
**Reset Value :** 0000h

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

MID3L [15:0]

**Register Offset:** 82h  
**Register Name:** MID3  
**Reset Value :** 0000h

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

MID3M [15:0]

**Register Offset:** 84h  
**Register Name:** MID3  
**Reset Value :** 0000h

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

MID3H [15:0]

The MAC/Multicast address MID3 [47:0] = {MID3H [15:0], MID3M [15:0], MID3L [15:0]};

**Bit 15-0: MID3L [15:0]**, the two bytes in the first line of the MAC/Multicast address.

**Bit 15-0: MID3M [15:0]**, the two bytes in the second line of the MAC/Multicast address.

**Bit 15-0: MID3H [15:0]**, the two bytes in the last line of the MAC/Multicast address.

## 21. DC Electrical Characteristics

### 21.1 Absolute Maximum Ratings (25 °C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
<b>DVCC/AVCC</b>	Supply Voltage	3.0	3.6	V	
<b>VIN</b>	DC Input Voltage (VIN)	3.0	3.6	V	
<b>VOUT</b>	DC Output Voltage (VOUT)	VCC-0.3	VCC+0.3	V	
<b>Vil</b>	Input Low Voltage	---	0.3xVCC	V	
<b>Vih</b>	Input High Voltage	0.7xVCC	---	V	
<b>Vol</b>	Output Low Voltage	---	0.4	V	
<b>Voh</b>	Output High Voltage	2.4	---	V	
<b>Iol*</b>	Switching Current Low	16VCC	---	mA	VCC>Vout 0.6VCC
<b>Ioh**</b>	Switching Current High	-12VCC	---	mA	0<Vout 0.3VCC

Note: \* Eq. C =  $(256/VCC) \times Vout \times (VCC - Vout)$

\*\* Eq. D =  $(98.0/VCC) \times (Vout - VCC) \times (Vout + 0.4VCC)$

### 21.2 Operating Temperature

Symbol	Parameter	Typ.	Unit	Conditions
<b>Tc</b>	Case Temperature	55~65		1. Ambient Temperature = 25 2. Open case testing.



## 22. AC Electrical Characteristics

### 22.1 Alphabetical Key to Switching Parameter Symbols

Parameter Symbol	No.	Description	Parameter Symbol	No.	Description
tAVCH	14	SAD Address Valid to Clock High	tCLDX	2	Data in Hold
tAVLL	12	SAD Address Valid to ALE Low	tCLR <sub>H</sub>	27	RD <sub>n</sub> Inactive Delay
tAVRL	66	SAD Address Valid to RD <sub>n</sub> Low	tCLRL	25	RD <sub>n</sub> Active Delay
tAVWL	65	SAD Address Valid to WR <sub>n</sub> Low	tDVCL	17	MCS <sub>n</sub> /PCS <sub>n</sub> Hold from Command Inactive
tAZRL	24	SAD Address Float to RD <sub>n</sub> Active	tDXDL	1	Data in Setup
tCHCSV	67	SD <sub>CLK</sub> High to LCS <sub>n</sub> /UCS <sub>n</sub> Valid	tLHLL	10	ALE Width
tCHCSX	18	MCS <sub>n</sub> /PCS <sub>n</sub> Inactive Delay	tLLAX	13	SAD Address Hold from ALE Inactive
tCHLH	9	ALE Active Delay	tRESIN	57	RST <sub>n</sub> Setup Time
tCHLL	11	ALE Inactive Delay	tRHAV	29	RD <sub>n</sub> Inactive to SAD Address Active
tCLAX	6	Address Hold	tRHDX	59	RD <sub>n</sub> High to Data Hold on SAD Bus
tCLAZ	15	SAD Address Float Delay	tRHLH	28	RD <sub>n</sub> Inactive to ALE High
tCLCSV	16	MCS/PCS Active Delay	tRLRH	26	RD <sub>n</sub> Pulse Width
tCLDV	7	Data Valid Delay	tWLWH	32	WR <sub>n</sub> Pulse Width

### 22.2 Numerical Key to Switching Parameter Symbols

No.	Parameter Symbol	Description	No.	Parameter Symbol	Description
1	tDVCL	Data in Setup	18	tCHCSX	MCS <sub>n</sub> /PCS <sub>n</sub> Inactive Delay
2	tCLDX	Data in Hold	24	tAZRL	SAD Address Float to RD <sub>n</sub> Active
6	tCLAX	Address Hold	25	tCLRL	RD <sub>n</sub> Active Delay
7	tCLDV	Data Valid Delay	26	tRLRH	RD <sub>n</sub> Pulse Width
9	tCHLH	ALE Active Delay	27	tCLR <sub>H</sub>	RD <sub>n</sub> Inactive Delay
10	tLHLL	ALE Width	28	tRHLH	RD <sub>n</sub> Inactive to ALE High
11	tCHLL	ALE Inactive Delay	29	tRHAV	RD <sub>n</sub> Inactive to SAD Address Active
12	tAVLL	SAD Address Valid to ALE Low	32	tWLWH	WR <sub>n</sub> Pulse Width
13	tLLAX	SAD Address Hold from ALE Inactive	57	tRESIN	RST <sub>n</sub> Setup Time
14	tAVCH	SAD Address Valid to Clock High	59	tRHDX	RD <sub>n</sub> High to Data Hold on SAD Bus
15	tCLAZ	SAD Address Float Delay	65	tAVWL	SAD Address Valid to WR <sub>n</sub> Low
16	tCLCSV	MCS/PCS Active Delay	66	tAVRL	SAD Address Valid to RD <sub>n</sub> Low
17	tCHCSX	MCS <sub>n</sub> /PCS <sub>n</sub> Hold from Command Inactive	67	tCHCSV	SD <sub>CLK</sub> High to LCS <sub>n</sub> /UCS <sub>n</sub> Valid

## 22.3 CPU Bus

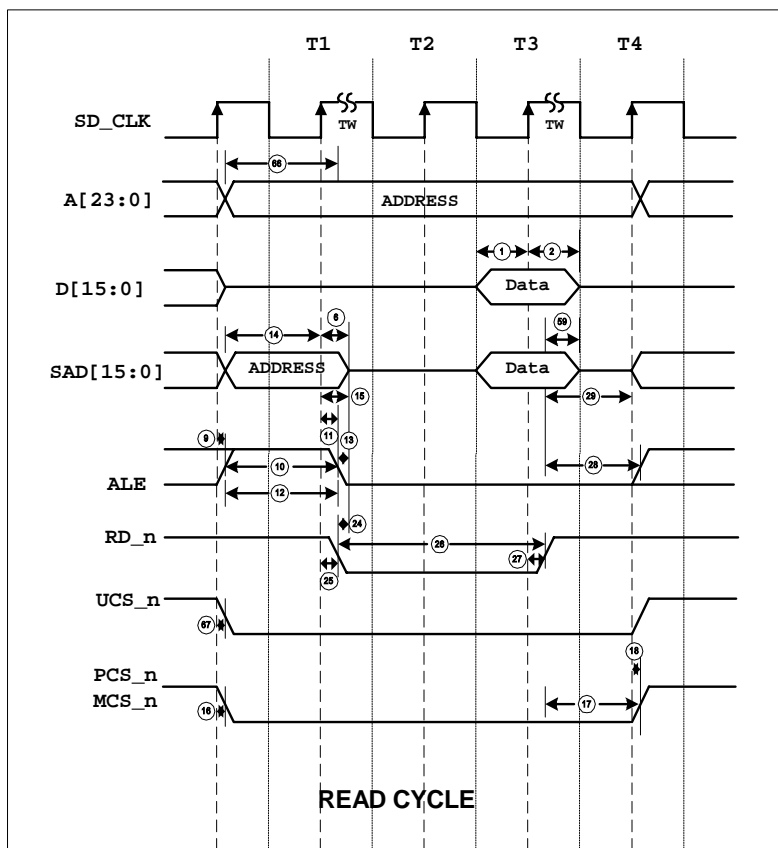
### Read Cycle (100 MHz)

Parameter			Preliminary		Unit
			100 MHz		
No.	Symbol	Description	Min.	Max.	
General Timing Requirements					
1	tDVCL	Data in Setup	2	---	ns
2	tCLDX	Data in Hold <sup>(c)</sup>	0.4	---	ns
General Timing Responses					
6	tCLAX	Address Hold	3	---	ns
9	tCHLH	ALE Active Delay	3	---	ns
10	tLHLL	ALE Width	1T	1.5T	ns
11	tCHLL	ALE Inactive Delay	---	2.7	ns
12	tAVLL	SAD Address Valid to ALE Low <sup>(a)</sup>	4.4 (T1+no wait)	9.2 (T1+wait)	ns
13	tLLAX	SAD Address Hold from ALE Inactive <sup>(a)</sup>	0.8	0.8+T1 wait	ns
14	tAVCH	SAD Address Valid to Clock High	---	1.2	ns
15	tCLAZ	SAD Address Float Delay	---	3.5	ns
16	tCLCSV	MCS_n/PCS_n Active Delay	8	---	ns
17	tcXCSX	MCS_n/PCS_n Hold from Command Inactive <sup>(a)</sup>	7	---	ns
18	tCHCSX	MCS_n/PCS_n Inactive Delay	5	---	ns
Read Cycle Timing Responses					
24	tAZRL	SAD Address Float to RD_n Active	---	0	ns
25	tCLRL	RD_n Active Delay	3	---	ns
26	tRLRH	RD_n Pulse Width	2T (0 wait)	2T+T3 wait	ns
27	tCLRHH	RD_n Inactive Delay	2.8	---	ns
28	trHLH	RD_n Inactive to ALE High <sup>(a)</sup>	4.5	---	ns
29	trHAV	RD_n Inactive to SAD Address Active <sup>(a)</sup>	6	---	ns
59	trHDX	RD_n High to Data Hold on SAD Bus <sup>(c)</sup>	0	---	ns
66	tAVRL	SAD Address Valid to RD_n Low <sup>(a)</sup>	---	14	ns
67	tCHCSV	SD_CLK High to UCS_n Valid	---	6	ns

**Notes:** All timing parameters are measured at 1.5 V with 50 pF loading on SD\_CLK unless otherwise noted. All output test conditions are with CL = 50 pF. For switching tests, VIL = 0.45 V and VIH = 2.4 V, except at X1 where VIH = VCC – 0.5 V.

- a. Equal loading on referenced pins. T1 wait states should be inserted to increase hold time.
- b. This parameter applies to the WR\_n, WHB\_n, and WLB\_n signals.
- c. If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

## Read Cycle Waveforms



**Write Cycle (100 MHz)**

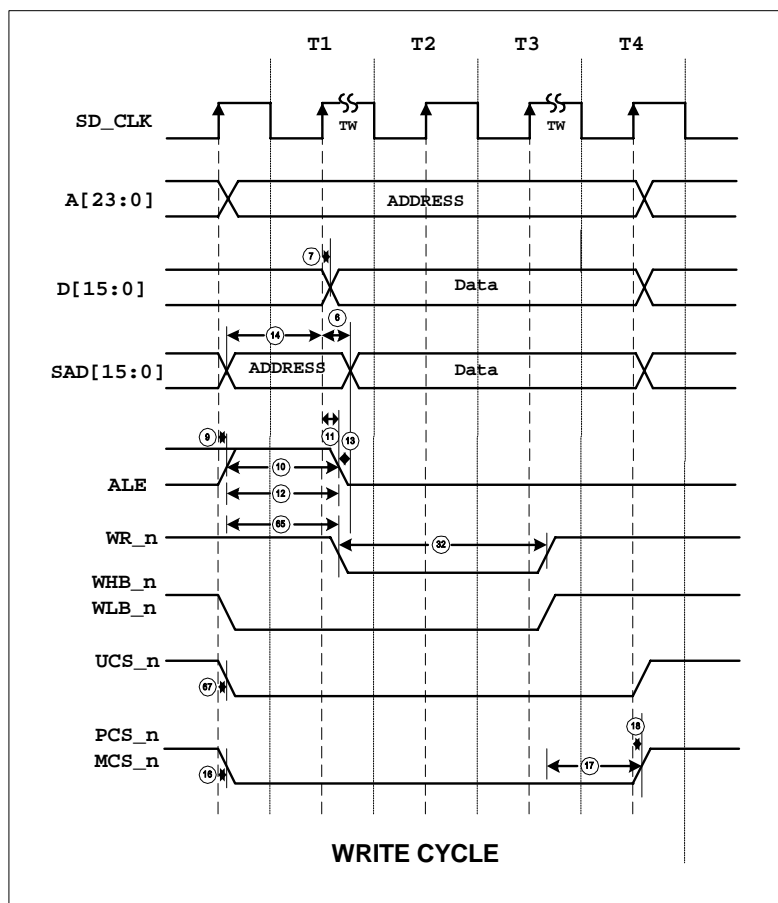
Parameter			Preliminary		Unit
			100 MHz		
No.	Symbol	Description	Min.	Max.	
General Timing Responses					
6	tCLAX	Address Hold	3	---	ns
7	tCLDV	Data Valid Delay	2.5	---	ns
9	tCHLH	ALE Active Delay	3	---	ns
10	tLHLL	ALE Width	1T	1.5T	ns
11	tCHLL	ALE Inactive Delay	---	2.7	ns
12	tAVLL	SAD Address Valid to ALE Low <sup>(a)</sup>	4.4 (T1 no wait)	9.2 (T1 wait)	ns
13	tLLAX	SAD Address Hold from ALE Inactive <sup>(a)</sup>	0.8 (T1 no wait)	5.6 (T1 wait)	ns
14	tAVCH	SAD Address Valid to Clock High	---	1.2	ns
16	tCLCSV	MCS_n/PCS_n Active Delay	8	---	ns
17	tcXCSX	MCS_n/PCS_n Hold from Command Inactive <sup>(a)</sup>	7	---	ns
18	tCHCSX	MCS_n/PCS_n Inactive Delay	5	---	ns
Write Cycle Timing Responses					
32	twLWH	WR_n Pulse Width	2T	2T+wait	ns
65	tAVWL	SAD Address Valid to WR_n Low	---	---	ns
67	tCHCSV	SD_CLK High to UCS_n Valid	---	6	ns

**Notes:** All timing parameters are measured at 1.5 V with 50 pF loading on SD\_CLK unless otherwise noted. All output test conditions are with CL = 50 pF. For switching tests, VIL = 0.45 V and VIH = 2.4 V, except at X1 where VIH = VCC – 0.5 V.

a. Equal loading on referenced pins. T1 wait states should be inserted to increase hold time.

b. This parameter applies to the WR\_n, WHB\_n, and WLB\_n signals.

### Write Cycle Waveforms

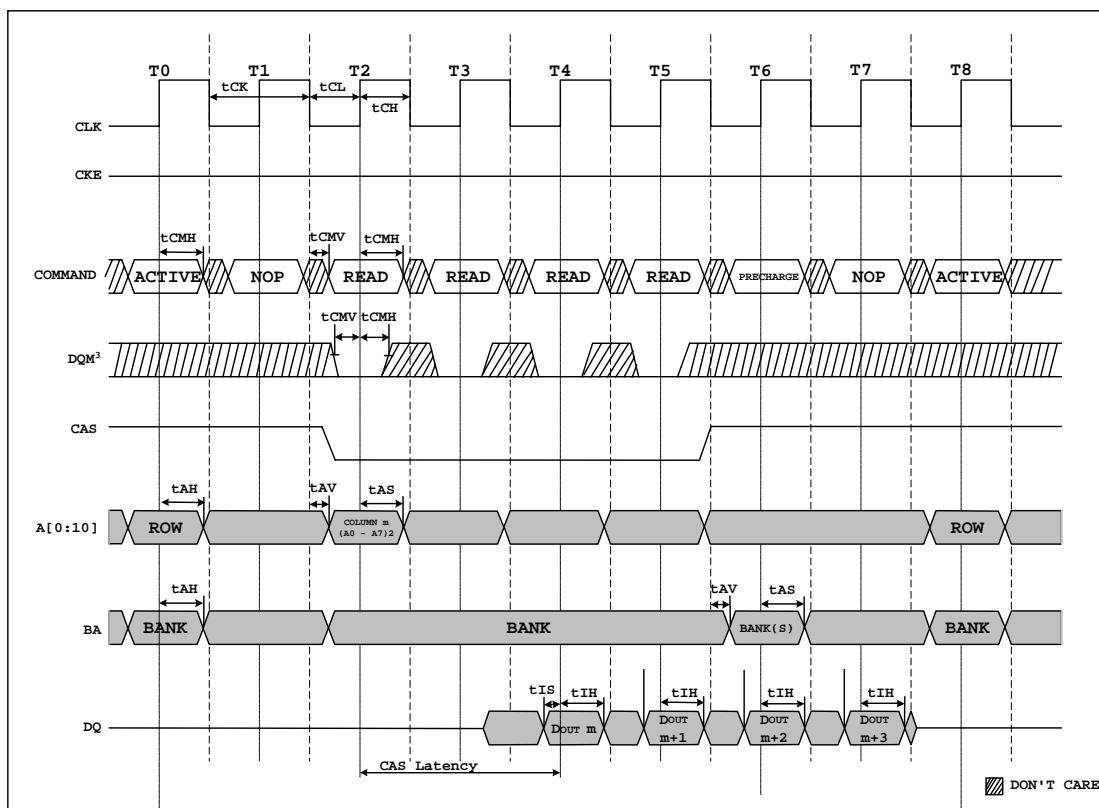


## 22.4 SDRAM Bus

### SDRAM Read Cycle (100 MHz)

Symbol	Description	Min.	Type	Max.
tCK	Clock Period time	10	---	---
tCL	Low Period time	---	5	---
tCH	Clock High Period time	---	5	---
TCMV	Command Valid Delay time	---	---	6
Tcmh	Command Hold time	4	---	---
TAv	Address Valid Delay time	---	---	5
tAH	Address Setup Hold time	4	---	---
tIS	Data Input Setup time	2	---	---
tIH	Data Input Hold time	1	---	---

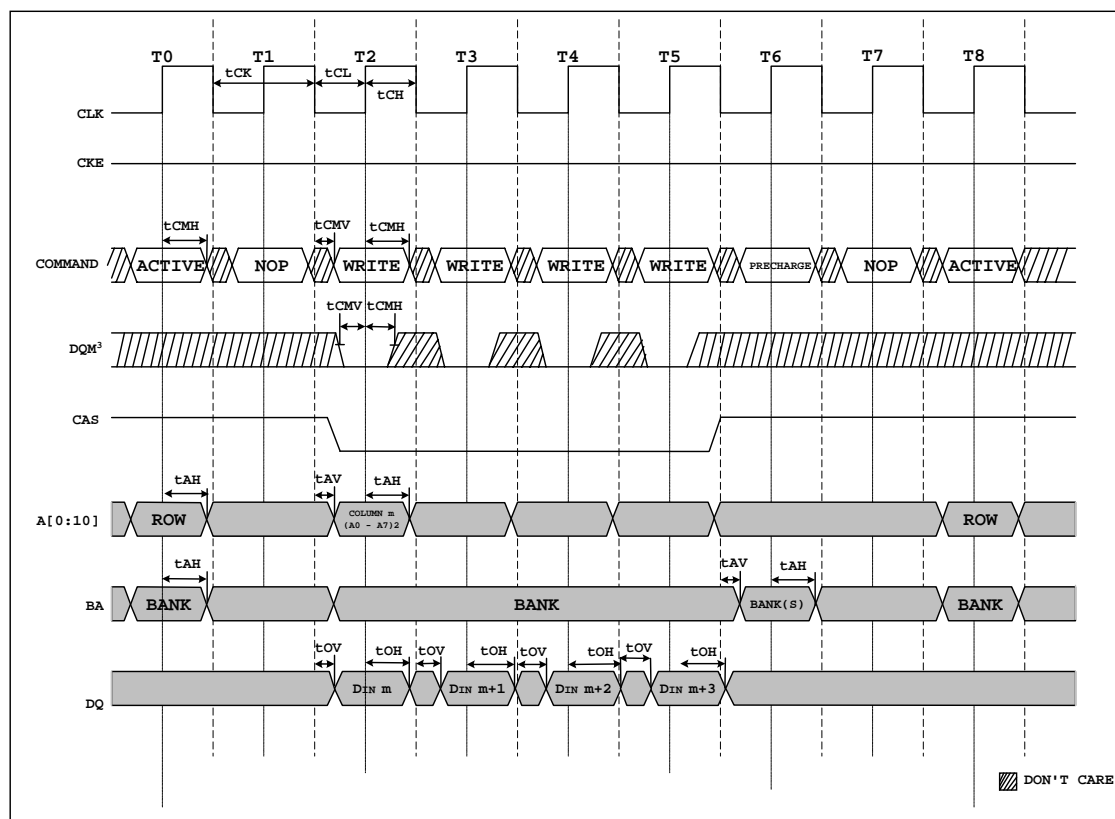
### SDRAM Read Cycle Waveforms



**SDRAM Write Cycle (100 MHz)**

Symbol	Description	Min.	Type	Max.
tCK	Clock Period time	10	---	---
tCL	Low Period time	---	5	---
tCH	Clock High Period time	---	5	---
tCMV	Command Valid Delay time	---	---	6
tCMH	Command Hold time	4	---	---
tAV	Address Valid Delay time	---	---	5
tAH	Address Setup Hold time	---	---	5
tOV	Data Output Valid Delay time	---	---	8
tOH	Data Output Hold time	0	---	---

**SDRAM Write Cycle Waveforms**



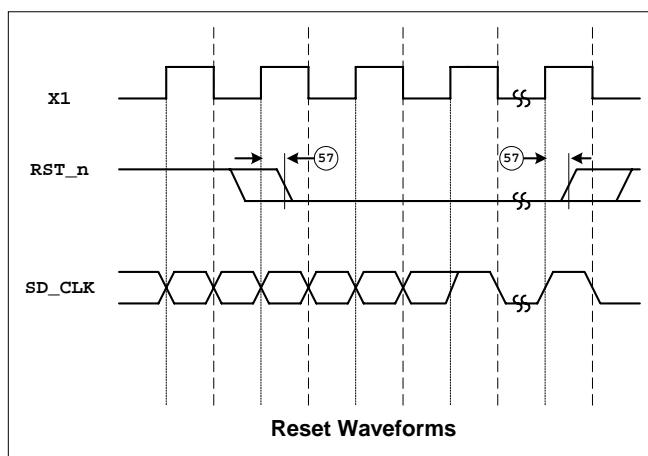
## 22.5 CPU Reset

### Reset and Bus Hold (100 MHz)

Parameter			Preliminary		Unit
			100 MHz		
No.	Symbol	Description	Min.	Max.	
Reset and Bus Hold Timing Requirements					
15	tCLAZ	SAD Address Float Delay	---	3.5	ns
57	tRESIN	RST_n Setup Time	2	---	ns

**Note:** All timing parameters are measured at 1.5 V with 50 pF loading on SD\_CLK unless otherwise noted. All output test conditions are with CL = 50 pF. For switching tests, V<sub>IL</sub> = 0.45 V and V<sub>IH</sub> = 2.4 V, except at X1 where V<sub>IH</sub> = V<sub>CC</sub> – 0.5 V.  
a. This timing must be met to guarantee recognition at the next clock.

### Reset Waveforms

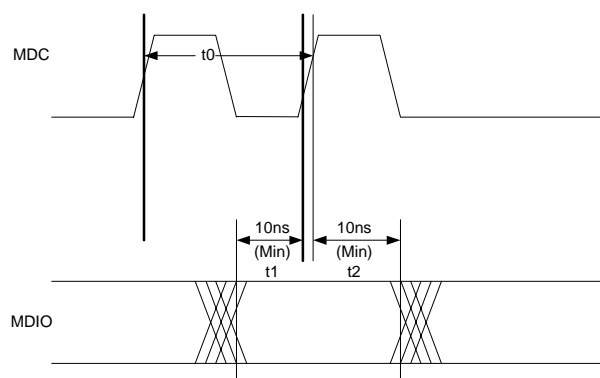




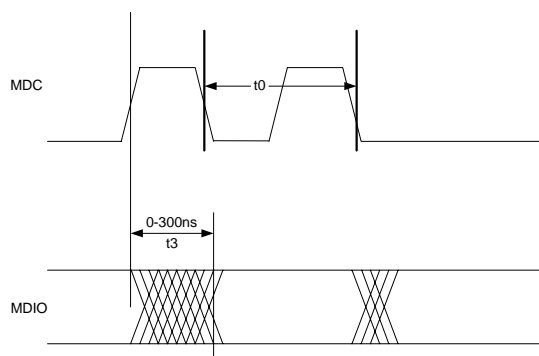
## 22.6 MDC/MDIO Timing

Symbol	Parameter	Min.	Type	Max.	Unit	Conditions
t0	MDC Cycle Time		TXC/10			
t1	MDIO Setup before MDC		MDC/2-10			
t2	MDIO Hold after MDC		MDC/2+10			
t3	MDC to MDIO Output Delay		10			

### MDIO Timing When OUTPUT by R2010C



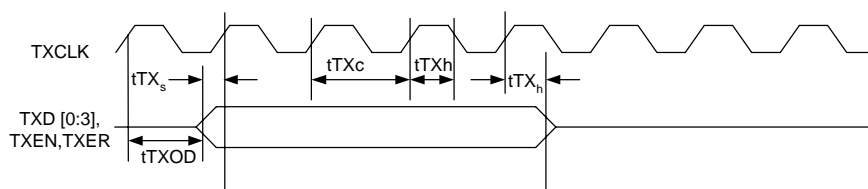
### MIDO Timing When OUTPUT by PHY



## 22.7 TX Transmit Timing Parameters

Symbol	Parameter	Min.	Type	Max.	Unit	Conditions
tTXh, tTXl	TXCLK High/Low Time					
tTXs	TXD{0:3}, TXEN, and TXER Setup to TXCLK High	1T-6				
tTXh	TXD{0:3}, TXEN, and TXER Hold from TXCLK High			4		
tTXOD	TXCLK to Output Delay			6		
Typical Values are at 25 °C and for design aid only; not guaranteed and not subject to production testing.						

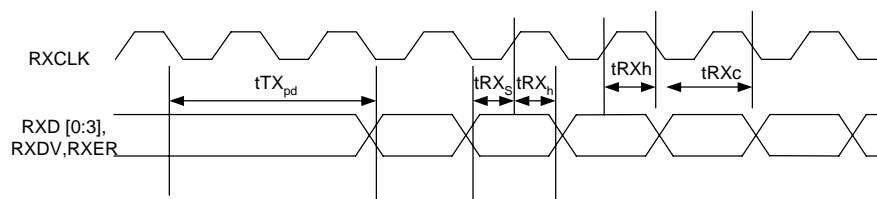
## 22.8 TX Transmit Timing Diagram



## 22.9 RX Receive Timing Parameters

Symbol	Parameter	Min.	Type	Max.	Unit	Conditions
tRXs	RXD{0:3}, RXDN, and RXER Setup to RXCLK High	0.8				
tRXh	RXD{0:3}, RXDN, and RXER Hold from RXCLK High	1				
Typical Values are at 25 °C and for design aid only; not guaranteed and not subject to production testing.						

## 22.10 RX Receive Timing Diagram



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## 23. Instruction Set OP-Code and Clock Cycles

Function	Format	Clocks	Notes
<b>DATA TRANSFER INSTRUCTIONS</b>			
<b>MOV = Move</b>			
register to register/memory	1000100w mod reg r/m	1/1	
register/memory to register	1000101w mod reg r/m	1/6	
immediate to register/memory	1100011w mod 000 r/m data data if w=1	1/1	
immediate to register	1011w reg data data if w=1	1	
memory to accumulator	1010000w addr-low addr-high	6	
accumulator to memory	1010001w addr-low addr-high	1	
register/memory to segment register	10001110 mod 0 reg r/m	3/8	
segment register to register/memory	10001100 mod 0 reg r/m	2/2	
<b>PUSH = Push</b>			
memory	11111111 mod 110 r/m	8	
register	01010 reg	3	
segment register	000reg110	2	
immediate	011010s0 data data if s=0	1	
<b>POP = Pop</b>			
memory	10001111 mod 000 r/m	8	
register	01011 reg	6	
segment register	000 reg 111 (reg 01)	8	
<b>PUSHA = Push all</b>	01100000	36	
<b>POPA = Pop all</b>	01100001	44	
<b>XCHG = Exchange</b>			
register/memory	1000011w mod reg r/m	3/8	
register with accumulator	10010 reg	3	
<b>XTAL = Translate byte to AL</b>	11010111	10	
<b>IN = Input from</b>			
fixed port	1110010w port	12	
variable port	1110110w	12	
<b>OUT = Output from</b>			
fixed port	1110010w port	12	
variable port	1110110w	12	
<b>LEA = Load EA to register</b>	10001101 mod reg r/m	1	
<b>LDS = Load pointer to DS</b>	11000101 mod reg r/m (mod 11)	14	
<b>LES = Load pointer to ES</b>	11000100 mod reg r/m (mod 11)	14	
<b>ENTER = Build stack frame</b>	11001000 data-low data-high L		
L = 0		7	
L = 1		11	
L > 1		11+10(L-1)	
<b>LEAVE = Tear down stack frame</b>	11001001	7	
<b>LAHF = Load AH with flags</b>	10011111	2	
<b>SAHF = Store AH into flags</b>	10011110	2	
<b>PUSHF = Push flags</b>	10011100	2	
<b>POPF = Pop flags</b>	10011101	11	
<b>ARITHMETIC INSTRUCTIONS</b>			
<b>ADD = Add</b>			

reg/memory with register to either	000000dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 000 r/m	data	data if sw=01	1/8	
immediate to accumulator	0000010w	data	data if w=1		1	
Function	Format				Clocks	Notes
ADC = Add with carry						
reg/memory with register to either	000100dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 010 r/m	data	data if sw=01	1/8	
immediate to accumulator	0001010w	data	data if w=1		1	
INC = Increment						
register/memory	1111111w	mod 000 r/m			1/8	
register	01000 reg				1	
SUB = Subtract						
reg/memory with register to either	001010dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 101 r/m	data	data if sw=01	1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
SBB = Subtract with borrow						
reg/memory with register to either	000110dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 011 r/m			1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
DEC = Decrement						
register/memory	1111111w	mod 001 r/m			1/8	
register	01001 reg				1	
NEG = Change sign						
register/memory	1111011w	mod reg r/m			1/8	
CMP = Compare						
register/memory with register	0011101w	mod reg r/m			1/7	
register with register/memory	0011100w	mod reg r/m			1/7	
immediate with register/memory	100000sw	mod 111 r/m	data	data if sw=01	1/7	
immediate with accumulator	0011110w	data	data if w=1		1	
MUL = multiply (unsigned)						
register-byte	1111011w	mod 100 r/m			13	
register-word					21	
memory-byte					18	
memory-word					26	
IMUL = Integer multiply (signed)						
register-byte	1111011w	mod 101 r/m			16	
register-word					24	
memory-byte					21	
memory-word					29	
register/memory multiply immediate (signed)	011010s1	mod reg r/m	data	data if s=0	23/28	
DIV = Divide (unsigned)						
register-byte	1111011W	mod 110 r/m			18	
register-word					26	
memory-byte					23	
memory-word					31	
IDIV = Integer divide (signed)						
register-byte	1111011w	mod 111 r/m			18	

register-word		26	
memory-byte		23	
memory-word		31	
<b>AAS</b> = ASCII adjust for subtraction	00111111	3	
<b>DAS</b> = Decimal adjust for subtraction	00101111	2	
<b>AAA</b> = ASCII adjust for addition	00110111	3	
<b>DAA</b> = Decimal adjust for addition	00100111	2	
<b>AAD</b> = ASCII adjust for divide	11010101	14	00001010
<b>AAM</b> = ASCII adjust for multiply	11010100	15	00001010
<b>CBW</b> = Corrvvert byte to word	10011000	2	
<b>CWD</b> = Convert word to double-word	10011001	2	

Function	Format	Clocks	Notes
<b>BIT MANIPULATION INSTRUCTUIONS</b>			
<b>NOT</b> = Invert register/memory	1111011w mod 010 r/m	1/7	
<b>AND</b> = And reg/memory and register to either immediate to register/memory immediate to accumulator	001000dw mod reg r/m 1000000w mod 100 r/m 0010010w data data if w=1	1/7 1/8 1	
<b>OR</b> = Or reg/memory and register to either immediate to register/memory immediate to accumulator	000010dw mod reg r/m 1000000w mod 001 r/m 0000110w data data if w=1	1/7 1/8 1	
<b>XOR</b> = Exclusive or reg/memory and register to either immediate to register/memory immediate to accumulator	001100dw mod reg r/m 1000000w mod 110 r/m 0011010w data data if w=1	1/7 1/8 1	
<b>TEST</b> = And function to flags , no result register/memory and register immediate data and register/memory immediate data and accumulator	1000010w mod reg r/m 1111011w mod 000 r/m 1010100w data data if w=1	1/7 1/8 1	
<b>Sifts/Rotates</b> register/memory by 1 register/memory by CL register/memory by Count	1101000w mod TTT r/m 1101001w mod TTT r/m 1100000w mod TTT r/m count	2/8 1+n / 7+n 1+n / 7+n	
<b>STRING MANIPULATION INSTRUCTIONS</b>			
<b>MOVS</b> = Move byte/word	1010010w	13	
<b>INS</b> = Input byte/word from DX port	0110110w	13	
<b>OUTS</b> = Output byte/word to DX port	0110111w	13	
<b>CMPS</b> = Compare byte/word	1010011w	18	
<b>SCAS</b> = Scan byte/word	101011w	13	
<b>LODS</b> = Load byte/word to AL/AX	1010110w	13	
<b>STOS</b> = Store byte/word from AL/AX	1010101w	7	
<b>Repeated by count in CX:</b>			
<b>MOVS</b> = Move byte/word	11110010 1010010w	4+9n	
<b>INS</b> = Input byte/word from DX port	11110010 0110110w	5+9n	
<b>OUTS</b> = Output byte/word to DX port	11110010 0110111w	5+9n	
<b>CMPS</b> = Compare byte/word	1111011z 1010011w	4+18n	
<b>SCAS</b> = Scan byte/word	1111001z 1010111w	4+13n	
<b>LODS</b> = Load byte/word to AL/AX	11110010 0101001w	3+9n	
<b>STOS</b> = Store byte/word from AL/AX	11110100 0101001w	4+3n	

## PROGRAM TRANSFER INSTRUCTIONS

**Conditional Transfers** — jump if:

**JE/JZ** = equal/zero

**JL/JNGE** = less/not greater or equal

**JLE/JNG** = less or equal/not greater

**JC/JB/JNAE** = carry/below/not above or equal

**JBE/JNA** = below or equal/not above

**JP/JPE** = parity/parity even

**JO** = overflow

**JS** = sign

**JNE/JNZ** = not equal/not zero

**JNL/JGE** = not less/greater or equal

**JNLE/JG** = not less or equal/greater

**JNC/JNB/JAE** = not carry/not below /above or equal

**JNBE/JA** = not below or equal/above

**JNP/JPO** = not parity/parity odd

**JNO** = not overflow

**JNS** = not sign

01110100	disp
01111100	disp
01111110	disp
01110010	disp
01110110	disp
01111010	disp
01110000	disp
01111000	disp
01110101	disp
01111101	disp
01111111	disp
01110011	disp
01110111	disp
01111011	disp
01110001	disp
01111001	disp

1/9

1/9

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1/9

### Function

### Format

### Clocks

### Notes

#### Unconditional Transfers

**CALL** = Call procedure

direct within segment

reg/memory indirect within segment

indirect intersegment

direct intersegment

11101000	disp-low	disp-high
11111111	mod 010 r/m	
11111111	mod 011 r/m	(mod 11)
10011010	segment offset	
	selector	

11

12/17

25

18

**RET** = Return from procedure

within segment

within segment adding immed to SP

intersegment

intersegment adding immed to SP

11000011		
11000010	data-low	data-high
11001011		
1001010	data-low	data-high

16

16

23

23

**JMP** = Unconditional jump

short/long

direct within segment

reg/memory indirect within segment

indirect intersegment

direct intersegment

11101011	disp-low	
11101001	disp-low	disp-high
11111111	mod 100 r/m	
11111111	mod 101 r/m	(mod ?11)
11101010	segment offset	
	selector	

9/9

9

11/16

18

11

#### Iteration Control

**LOOP** = Loop CX times

**LOOPZ/LOOPE** = Loop while zero/equal

**LOOPNZ/LOOPNE** = Loop while not zero/equal

**JCXZ** = Jump if CX = zero

11100010	disp
11100001	disp
11100000	disp
11100011	disp

7/16

7/16

7/16

7/15

#### Interrupt

**INT** = Interrupt

Type specified

11001101	type
----------	------

41

Type 3	11001100		41	
<b>INTO</b> = Interrupt on overflow	11001110		43/4	
<b>BOUND</b> = Detect value out of range	01100010	mod reg r/m	21-60	
<b>IRET</b> = Interrupt return	11001111		31	
<b>PROCESSOR CONTROL INSTRUCTIONS</b>				
<b>CLC</b> = clear carry	11111000		2	
<b>CMC</b> = Complement carry	11110101		2	
<b>STC</b> = Set carry	11111001		2	
<b>CLD</b> = Clear direction	11111100		2	
<b>STD</b> = Set direction	11111101		2	
<b>CLI</b> = Clear interrupt	11111010		5	
<b>STI</b> = Set interrupt	11111011		5	
<b>HLT</b> = Halt	11110100		1	
<b>WAIT</b> = Wait	10011011		1	
<b>LOCK</b> = Bus lock prefix	11110000		1	
<b>ESC</b> = Math coprocessor escape	11011MMM	mod PPP r/m	1	
<b>NOP</b> = No operation	10010000		1	
<b>SEGMENT OVERRIDE PREFIX</b>				
CS	00101110		2	
SS	00110110		2	
DS	00111110		2	
ES	00100110		2	

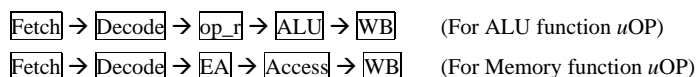
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## 24. R2010C Execution Timing

The above instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

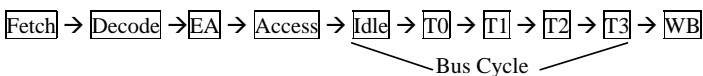
1. The opcode, along with data or displacement required for execution, has been prefetched and resided in the instruction queue at the time needed.
2. No wait states or bus HOLDS occur.
3. All word -data are located on even-address boundaries.
4. One RISC micro operation (*uOP*) maps one cycle (according to the pipeline stages described below), except the following case:

Pipeline Stages for single micro operation(one cycle):



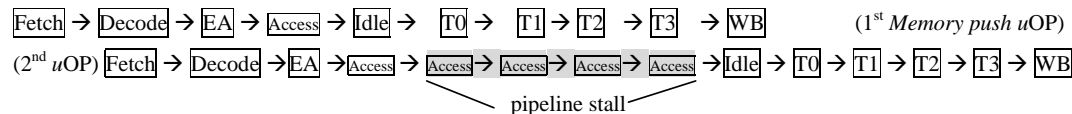
4.1 *Memory read uOP* need 6 cycles for bus.

Pipeline stages for *Memory read uOP*(6 cycles):



4.2 *Memory push uOP* need 1 cycle if it has no previous *Memory push uOP*, and 5 cycles if it has previous *Memory push* or *Memory Write uOP*.

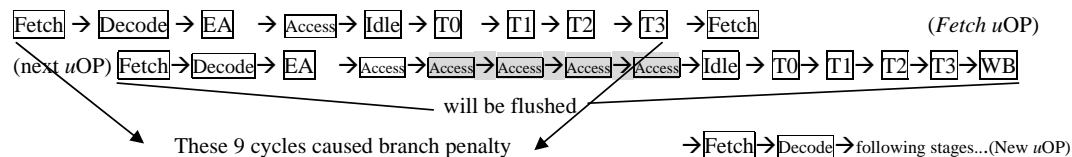
Pipeline stages for *Memory push uOP* after *Memory push uOP* (another 5 cycles):



4.3 *MUL uOP* and *DIV* of ALU function *uOP* for 8 bits operation need both 8 cycles, for 16 bits operation need both 16 cycles.

4.4 All jumps, calls, ret and loopXX instructions required to fetch the next instruction for the destination address (*Unconditional Fetch uOP*) will need 9 cycles.

Pipeline stages for unconditional fetch:



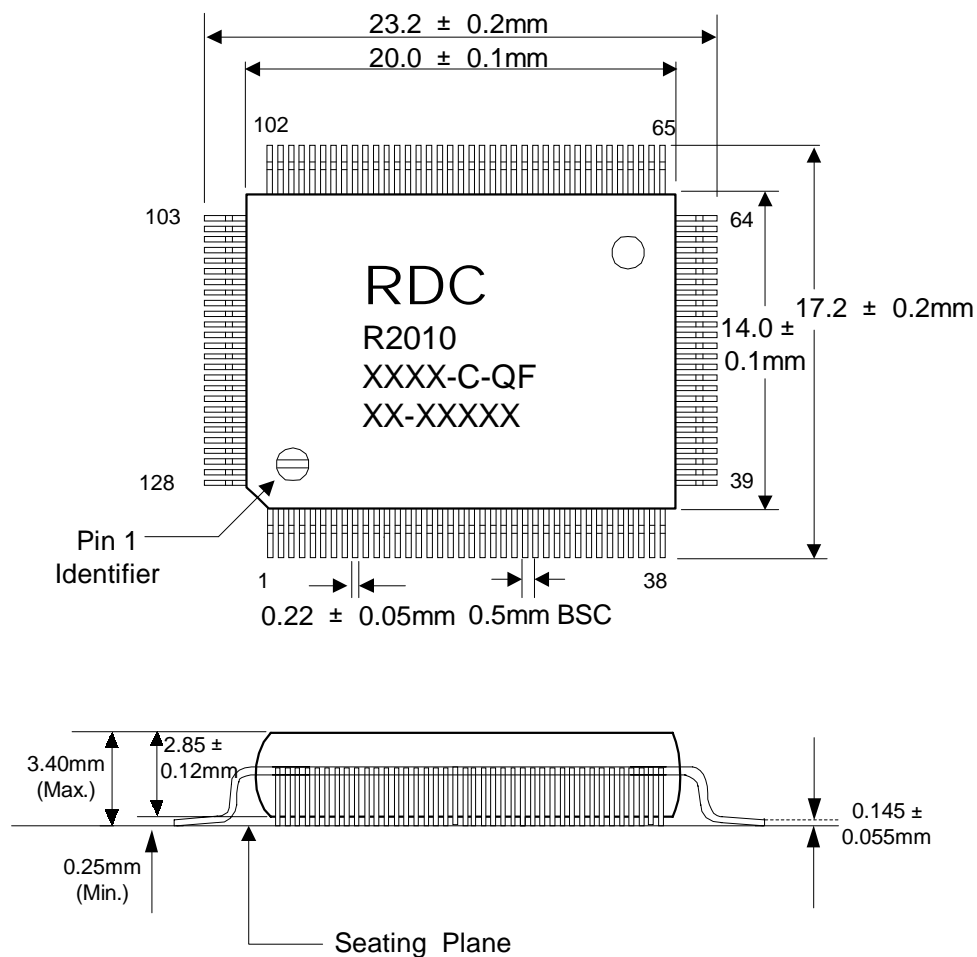
**Note:** op\_r: operand read stage, EA: Calculate Effective Address stage, Idle: Bus Idle stage, T0..T3: Bus T0..T3 stage,

Access: Access data from cache memory stage.



## 25. Package Information

### 25.1 PQFP 128 pins



## 26. Revision History

Rev.	Date	History
D01	12/17/2002	Draft Version 0.1
D02	12/31/2002	Draft Version 0.2
P01	01/23/2003	Preliminary Version 0.1
P02	02/11/2003	Preliminary Version 0.2
F10	02/17/2003	Final Version 1.0
F11	03/18/2003	Final Version 1.1 1. page 13 (Pin 12 & 13): the third line from bottom The INT6/5 are edge-triggered only and must be held until the interrupt is acknowledged. = > The INT6/5 are <b>level-triggered</b> only. 2. page 39: Insert one paragraph of descriptions for A6h register. 3. page 99: Bit 6 & 5 for F4h register are modified to be <b>Reserved</b> .