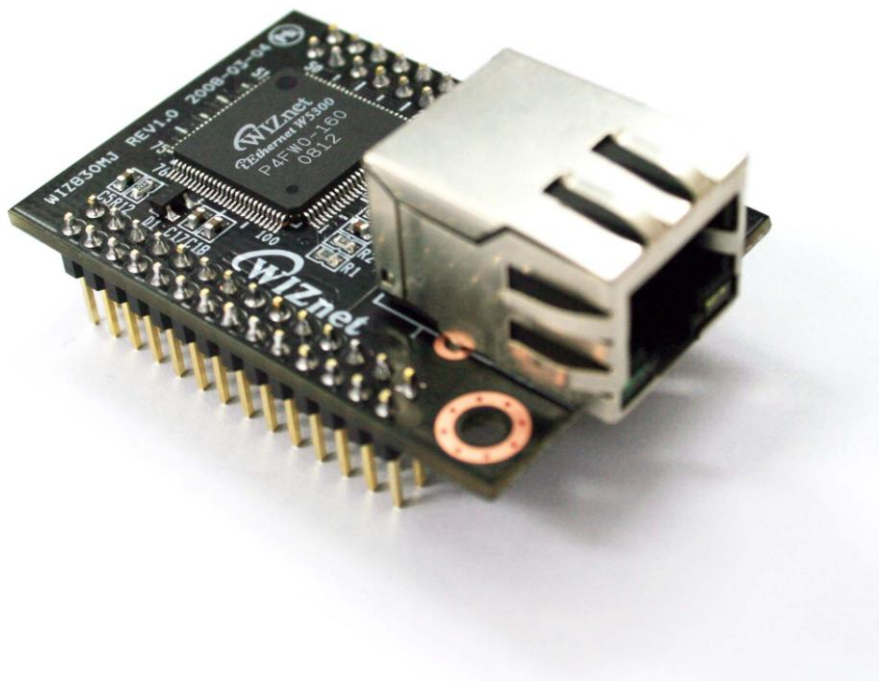


# WIZ830MJ Datasheet

(Ver. 1.2)



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## Document History Information

| Revision | Data          | Description                                  |
|----------|---------------|--|
| Ver.1.0  | June 04, 2008 | Release with WIZ830MJ Launching              |
| Ver.1.1  | July 29, 2008 | Modified dimensions(Symbol B and C).         |
| Ver.1.2  | March 4, 2010 | Pin number of A[9:0] modified in Chapter 2.3 |

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If you have something to ask about WIZnet Products, Write down your question on Q&A Board in WIZnet website ([www.wiznet.co.kr](http://www.wiznet.co.kr)). WIZnet Engineer will give an answer as soon as possible.

The screenshot shows the WIZnet website homepage. At the top, there is a navigation bar with links for HOME, LOGIN, JOIN, CONTACT US, and language options (ENGLISH, CHINESE, JAPANESE, KOREAN). A search bar for 'On-line Mail' is also present. A main navigation menu on the left includes: PRODUCTS, TECHNOLOGY, TECHNICAL Q&A (highlighted), LIBRARY, DISTRIBUTOR, PARTNERSHIP, BLOG, and ABOUT US. A secondary menu includes Q&A, FAQ, and E-FORUM. The central banner features a WIZnet W5300 Ethernet chip with the text 'Stable 70Mbps Guaranteed (in DMA!) W5300'. To the right, a 'WIZnet website Renewal/Open with web 2.0 concepts!' box lists updates: Easy-to-check new or amended info, Support RSS, Enhanced Search function, Open Blog & Community menu, Build Technical forum, Easy-to-find local distributors, WIZnet's innovation spirit, Chinese version Grand Open, and Japanese version Coming Soon. Below the banner, there are sections for 'RoHS Compliant', 'NEW PRODUCT W5300' (listing features like 50 Mbps, 16/8 bit bus, 8 sockets, and SWTCP/IP), and 'WHAT'S UPDATED' (listing firmware and driver updates). A footer contains 'COMPANY OVERVIEW', 'DISTRIBUTOR', and various event announcements like 'WIZnet 3rd Party e-market place', 'WIZnet e-sale International', '2007 WIZnet Ethernet Winners Announcement', and 'IIC Taiwan Sep. 9-11, 2008 Booth #: 2L06'.

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# 1. Introduction

WIZ830MJ is the network module that includes W5300 (TCP/IP hardwired chip, include PHY), MAG-JACK (RJ45 with X'FMR) with other glue logics. It can be used as a component and no effort is required to interface W5300 and Transformer. The WIZ830MJ is an ideal option for users who want to develop their Internet enabling systems rapidly.

**For the detailed information on implementation of Hardware TCP/IP, refer to the W5300 Datasheet.**

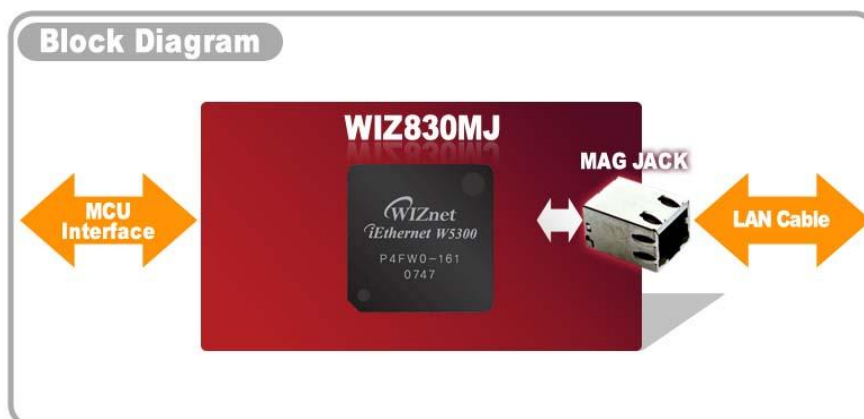
WIZ830MJ consists of W5300 and MAG-JACK.

- TCP/IP, MAC protocol layer: W5300
- Physical layer: Included in W5300
- Connector: MAG-JACK(RJ45 with Transformer)

## 1.1. Features

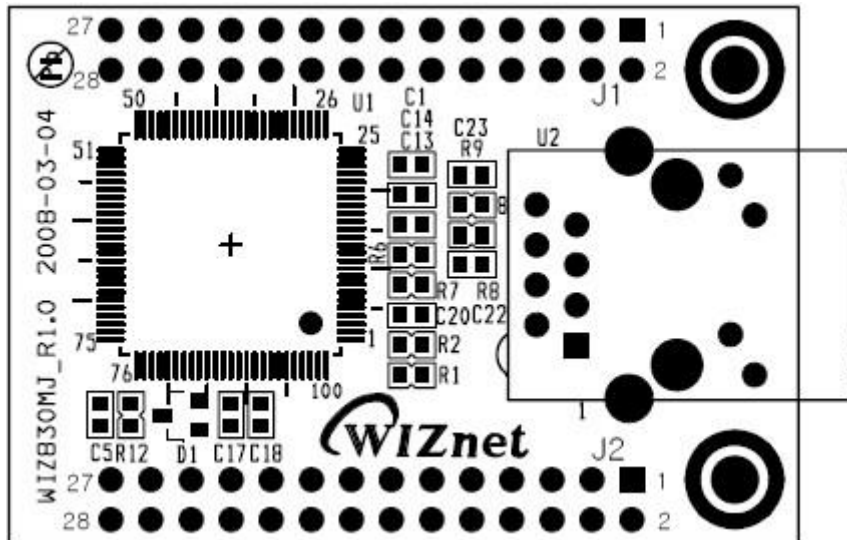
- Supports 10/100 Base TX
- High network performance : Up to 50Mbps
- Supports half/full duplex operation
- Supports auto-negotiation and auto cross-over detection
- IEEE 802.3/802.3u Compliance
- Operates 3.3V with 5V I/O signal tolerance
- Supports network status indicator LEDs
- Includes Hardware Internet protocols: TCP, IP Ver.4, UDP, ICMP, ARP, PPPoE, IGMP
- Includes Hardware Ethernet protocols: DLC, MAC
- Supports 8 independent connections simultaneously
- Supports MCU bus Interface
- Supports Direct/Indirect mode bus access
- Supports 16/8 bit data bus width
- Supports memory-to-memory DMA (only 16bit Data bus width & slave mode)
- Supports Socket API for easy application programming
- Supports hybrid TCP/IP stack(software and hardware TCP/IP stack)
- Supports PPPoE connection (with PAP/CHAP Authentication mode)
- More flexible allocation internal TX/RX memory according to application throughput
- Interfaces with two 2.54mm pitch 2 x 14 header pin

## 1.2. Block Diagram



## 2. Pin Assignments & descriptions

### 2.1. Pin Assignments



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| J1  |    |    |     | J2       |    |    |         |
|-----|----|----|-----|----------|----|----|---------|
| VCC | 1  | 2  | D15 | VCC      | 1  | 2  | BIT16EN |
| D14 | 3  | 4  | D13 | /LINKLED | 3  | 4  | /TXLED  |
| D12 | 5  | 6  | D11 | /RXLED   | 5  | 6  | /COLLED |
| D10 | 7  | 8  | D9  | /FDXLED  | 7  | 8  | /SPDLED |
| D8  | 9  | 10 | D7  | /ACTLED  | 9  | 10 | GND     |
| D6  | 11 | 12 | D5  | BRDY3    | 11 | 12 | BRDY2   |
| D4  | 13 | 14 | D3  | BRDY1    | 13 | 14 | BRDY0   |
| D2  | 15 | 16 | D1  | GND      | 15 | 16 | GND     |
| D0  | 17 | 18 | GND | /RESET   | 17 | 18 | /INT    |
| A9  | 19 | 20 | A8  | /CS      | 19 | 20 | /RD     |
| A7  | 21 | 22 | A6  | /WR      | 21 | 22 | NC      |
| A5  | 23 | 24 | A4  | GND      | 23 | 24 | GND     |
| A3  | 25 | 26 | A2  | NC       | 25 | 26 | NC      |
| A1  | 27 | 28 | A0  | NC       | 27 | 28 | NC      |

I : Input  
I/O : Bi-directional Input and output

O : Output  
P : Power

## 2.2. Power & Ground

| Symbol | Type | Pin No.                                     | Description                |
|--------|------|---|----------------------------|
| VCC    | P    | J1:1, J2:1                                  | Power : 3.3 V power supply |
| GND    | P    | J1:18, J2:10, J2:15,<br>J2:16, J2:23, J2:24 | Ground                     |

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## 2.3. MCU Interfaces

| Symbol  | Type | Pin No.       | Description   |
|---------|------|---------------|---|
| A[9:0]  | I    | J1:19 ~ J1:28 | <b>Address</b><br>Used as Address[9-0] pin  |
| D[15:8] | I/O  | J1:2 ~ J1:9   | <b>Data</b><br>16 bit-wide high data bus<br>In case of using 8 bit data bus, there are driven as High-Z   |
| D[7:0]  | I/O  | J1:10 ~ J1:17 | <b>Data</b><br>16 bit-wide low data bus   |
| /CS     | I    | J2:19         | <b>Module Select</b> : Active low.<br>/CS of W5300  |
| /RD     | I    | J2:20         | <b>Read Enable</b> : Active low.<br>/RD of W5300  |
| /WR     | I    | J2:21         | <b>Write Enable</b> : Active low<br>/WR of W5300  |
| /INT    | O    | J2:18         | <b>Interrupt</b> : Active low<br>After reception or transmission it indicates that the W5300 requires MCU attention.<br>By writing values to the Interrupt Register(IR) of W5300 the interrupt will be cleared by host.<br>All interrupts can be masked by writing values to the IMR of W5300 (Interrupt Mask Register).<br>For more details refer to the W5300 Datasheet |
| BIT16EN | I    | J2:2          | <b>16/8 bit data bus select.</b><br>High : 16 bit data bus<br>Low : 8 bit data bus.   |

## 2.4. Network Indicator LED Signals

| Symbol   | Type | Pin No. | Description   |
|----------|------|---------|---|
| /LINKLED | O    | J2:3    | <b>Link LED</b><br>It indicates the link status of media(10/100M).  |
| /TXLED   | O    | J2:4    | <b>Transmit activity LED : Transmit Enable</b><br>It notifies the output of transmit data through TXOP/TXON (Transmit Activity).  |
| /RXLED   | O    | J2:5    | <b>Receive activity LED : Transmit Data</b><br>It notifies the input of receive data from RXIP/RXIN (Receive Activity)  |
| /COLLED  | O    | J2:6    | <b>Collision LED : Transmit Data</b><br>It notifies when collisions occur. It is valid at half-duplex, and is ignored at full-duplex.   |
| /FDXLED  | O    | J2:7    | <b>Full duplex LED : Transmit Data</b><br>It outputs low at the full-duplex and outputs high at the halfduplex according to auto-negotiation or manual configuration of OP_MODE[2:0]. |
| /SPDLED  | O    | J2:8    | <b>Link speed LED : Transmit Data</b><br>It is asserted low at the 100Mbps and high at the 10Mbps according to auto-negotiation or manual configuration of OP_MODE[2:0].              |
| /ACTLED  | O    | J2:9    | <b>Activity LED</b><br>It notifies the output of transmit data through TXOP/TXON or the input of receive data from RXIP/RXIN.   |

## 2.5. Miscellaneous Signals

| Symbol    | Type | Pin No.                             | Description   |
|-----------|------|-------------------------------------|---|
| /RESET    | I    | J2:17                               | <b>Reset</b> : This pin is active low input to initialize or re-initialize W5300. RESET should be held at least 2us after low assert, and wait for at least 10ms after high de-assert in order for PLL logic to be stable |
| BRDY[3:0] | O    | J2:11 ~ J2:14                       | <b>Buffer Ready Indicator</b><br>BRDYn monitors TX/RX memory status of each socket. For more details refer to the W5300 Datasheet   |
| NC        | -    | J2 : 22, J2:25, J2:26, J2:27, J2:28 | Not Connect   |

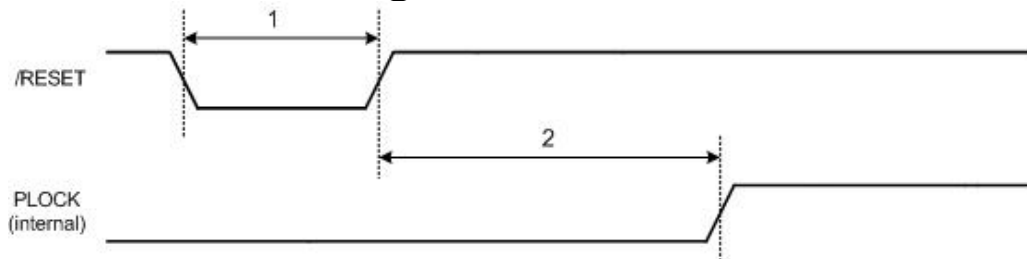


## 3. Timing Diagrams

WIZ830MJ provides following interfaces of W5300.

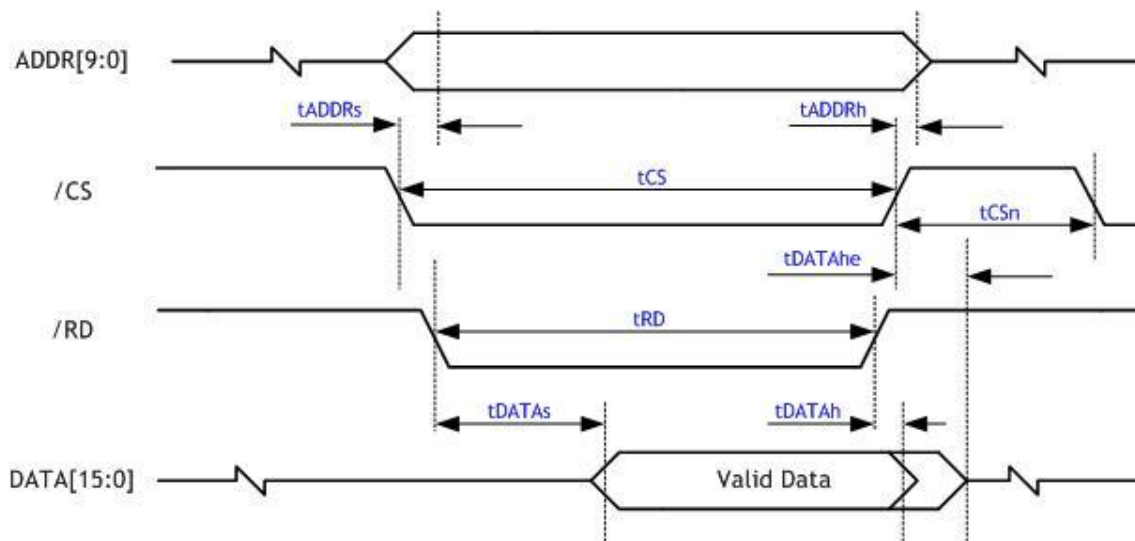
-. Direct/Indirect mode bus access

### 3.1. Reset Timing



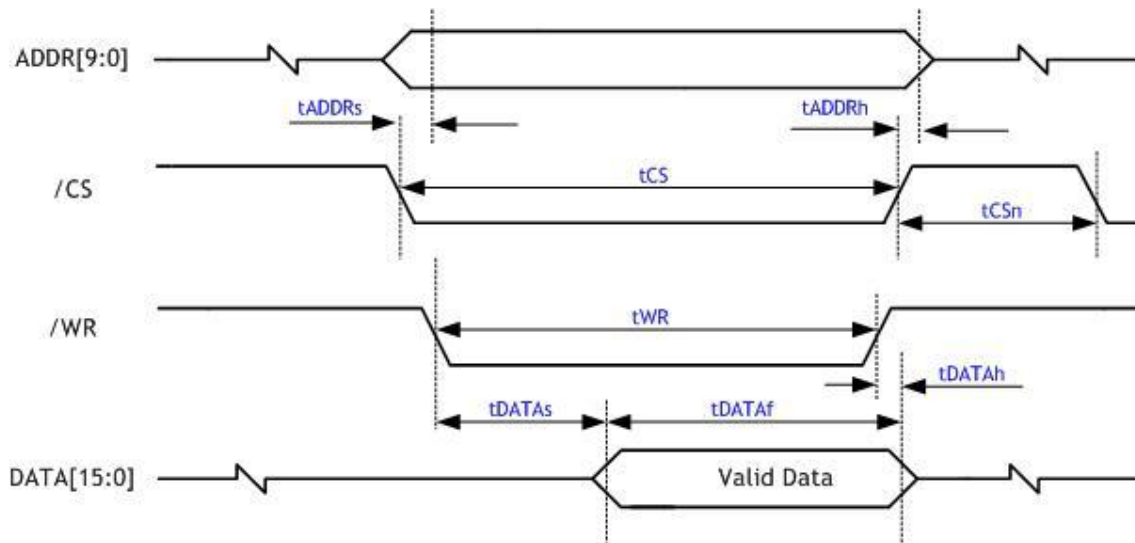
| Description |                  | Min  | Max  |
|-------------|------------------|------|------|
| 1           | Reset Cycle Time | 2 us | -    |
| 2           | PLL Lock-in Time | 50us | 10 s |

### 3.2. Register / Memory READ Timing



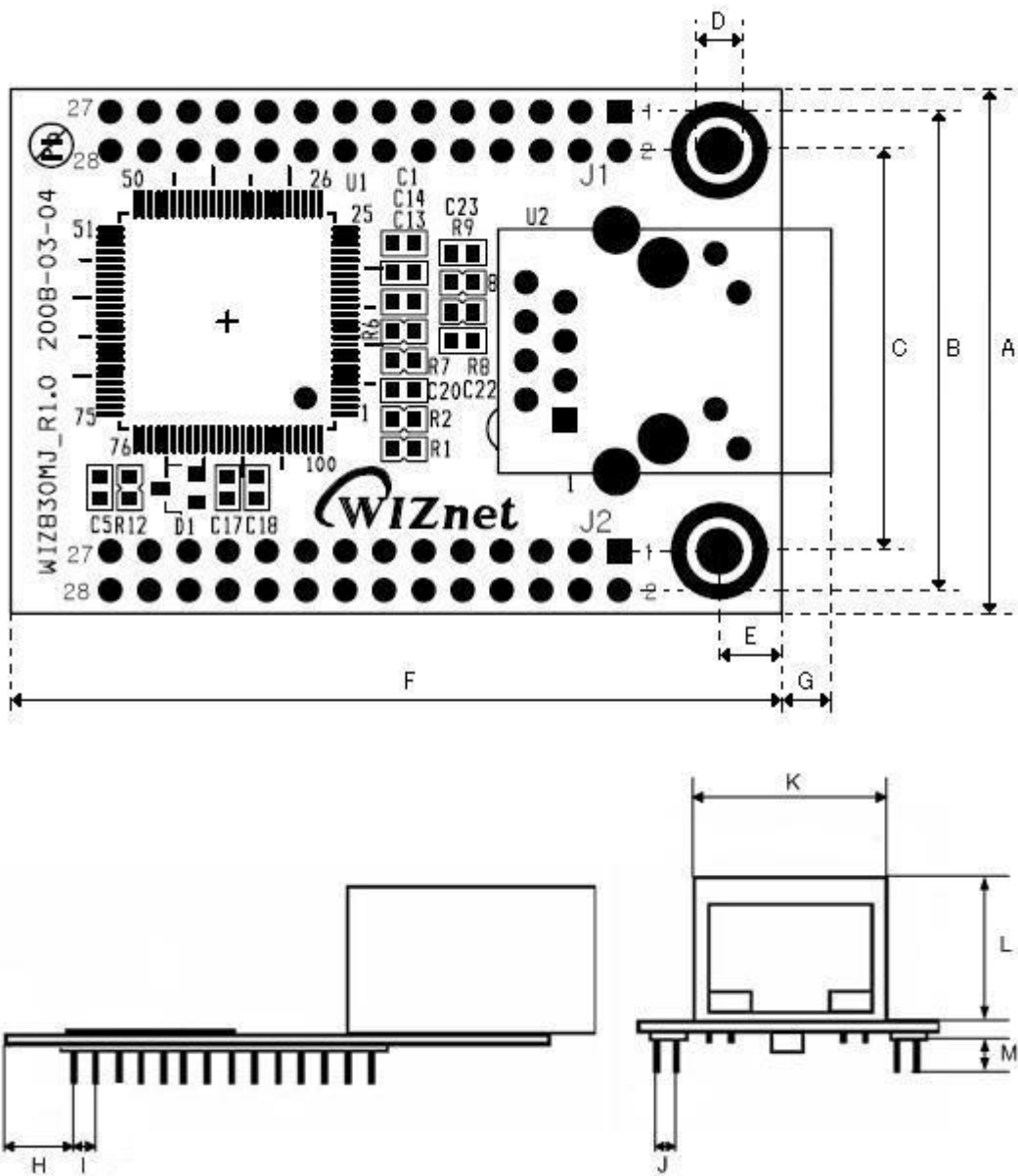
| Description |  | Min  | Max       |
|-------------|--|------|-----------|
| tADDRs      | Address Setup Time after /CS and /RD low | -    | 7ns       |
| tADDRh      | Address Hold Time after /CS and /RD high | -    | -         |
| tCS         | /CS Low Time                             | 65ns | -         |
| tCSn        | /CS Next Assert Time                     | 28ns | -         |
| tRD         | /RD Low Time                             | 65ns | -         |
| tDATAs      | DATA Setup Time after /RD low            | 42ns | -         |
| tDATAh      | DATA Hold Time after /RD and /CS high    | -    | 7ns       |
| tDATAhe     | DATA Hold Extension Time after /CS high  | -    | 2XPLL_CLK |

### 3.3. Register / Memory WRITE Timing



| Description |  | Min  | Max                  |
|-------------|--|------|----------------------|
| $t_{ADDRs}$ | Address Setup Time after /CS and /WR low | -    | 7ns                  |
| $t_{ADDRh}$ | Address Hold Time after /CS or /RD high  | -    | -                    |
| $t_{CS}$    | /CS low Time                             | 50ns | -                    |
| $t_{CSn}$   | /CS next Assert Time                     | 28ns |                      |
| $t_{WR}$    | /WR low Time                             | 50ns |                      |
| $t_{DATAs}$ | Data Setup Time after /WR low            | 7ns  | $7ns + 7XPLL\_CLK$   |
| $t_{DATAf}$ | Data Fetch Time                          | 14ns | $t_{WR} - t_{DATAs}$ |
| $t_{DATAh}$ | Data Hold Time after /WR high            | 7ns  | -                    |

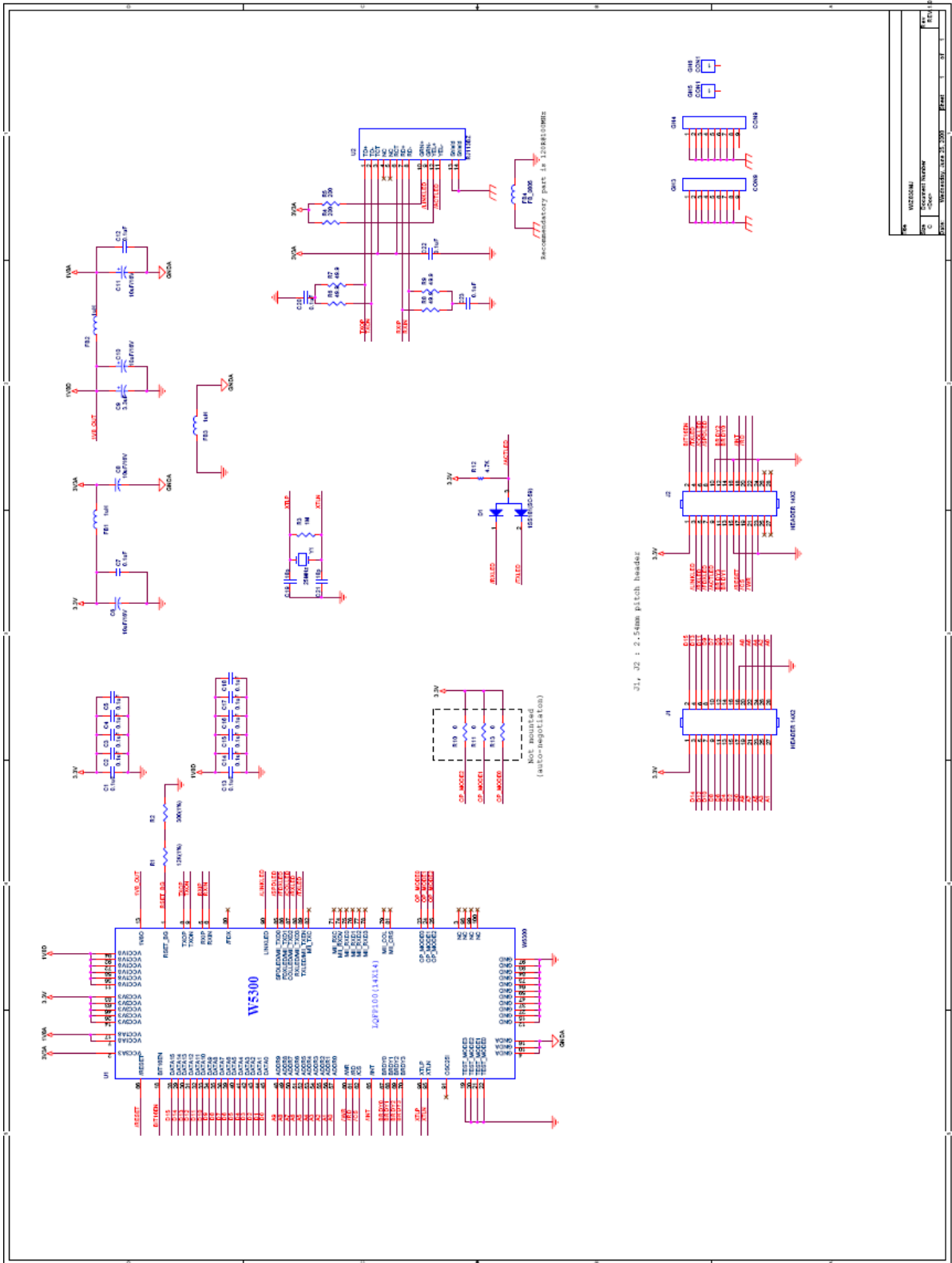
## 4. Dimensions



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| Symbols | Dimensions (mm) | Symbols | Dimensions (mm) |
|---------|-----------------|---------|-----------------|
| A       | 34.00           | H       | 6.50            |
| B       | 30.48           | I       | 2.54            |
| C       | 25.40           | J       | 2.54            |
| D       | 3.00            | K       | 15.90           |
| E       | 4.00            | L       | 13.50           |
| F       | 50.00           | M       | 6.00            |
| G       | 3.30            | -       | -               |

# 5. Schematic



|     |                   |            |        |
|-----|-------------------|------------|--------|
| REV | DESCRIPTION       | DATE       | BY     |
| 1.0 | WIZ830MJ_V1.0_000 | 2008.08.20 | WIZnet |

## 6. Partlists

| Item | Q.ty | Reference   | Part                                     | Tech. Characteristics  | Package       |
|------|------|---|--|------------------------|---------------|
| 1    | 16   | C1,C2,C3,C4,C5,<br>C7,C12,C13,C14,<br>C15,C16,C17,C18,<br>C20,C22,C23 | 0.1uF                                    | 50V-20% Ceramic        | CASE 0603     |
| 2    | 4    | C6,C8,C10,C11,  | 10uF/16V                                 | 16Vmin 10%             | EIA/IECQ 3216 |
| 3    | 1    | C9  | 3.3uF/16V                                | 16Vmin 10%             | EIA/IECQ 3216 |
| 4    | 2    | C19,C21   | 18pF                                     | 50V-20% Ceramic        | CASE 0603     |
| 5    | 1    | D1  | 1SS181                                   |                        | SC-59         |
| 6    | 3    | FB1,FB2,FB3   | 1uH<br>Chip Ferrite Inductor             | 1uH, 50mA              | CASE 0805     |
| 7    | 1    | FB4   | 120 Ohm Ferrite BEAD                     | 120 Ohm /100MHz        | CASE 0805     |
| 8    | 2    | J1,J2   | 2X14 28PIN 2.54mm<br>DIP STRAIGHT Header | 2 X 14 2.54mm pitch    | DIP           |
| 9    | 1    | R1  | 12K (1%)                                 | 1/10W-1% SMD           | CASE 0603     |
| 10   | 1    | R2  | 300 (1%)                                 | 1/10W-1% SMD           | CASE 0603     |
| 11   | 1    | R3  | 1M                                       | 1/10W-5% SMD           | CASE 0603     |
| 12   | 2    | R4,R5   | 200                                      | 1/10W-5% SMD           | CASE 0603     |
| 13   | 4    | R6,R7,R8,R9   | 49.9 (1%)                                | 1/10W-1% SMD           | CASE 0603     |
| 14   | 0    | R10,R11,R13   | Not mounted                              | 1/10W-5% SMD           | CASE 0603     |
| 15   | 1    | R12   | 4.7K                                     | 1/10W-5% SMD           | CASE 0603     |
| 16   | 1    | U1  | W5300                                    | WIZnet Hardware TCP/IP | LQFP100       |
| 17   | 1    | U2  | RJ113BZ                                  | Transformer + RJ-45    |               |
| 18   | 1    | Y1  | 25MHz(SMD)                               | SMD Type, CL=18pF      | SX-1          |
| 19   | 1    |   | WIZ830MJ REV1.0 PCB                      | 1.6T 4LAYER            |               |