POWERTIP TECH. CORP.

SPECIF IC ATIONS

CUSTOMER	:	CCN026
SAMPLE CODE (Ver.)	:	PS240320T-030-X-03 (Ver.0)
MASS PRODUCTION CODE (Ver.)	:	PH240320T-030-XP1Q (Ver.A)
DRAWING NO. (Ver.)	:	TE-240320037 (Ver.0)

Customer Approved

Date:

JAN 23 2008 R&D APPROVED

Approved	QC Confirmed	Designer
	QA.DEPT 2008 1. 23 POWERTIP	

■ Approval For Specifications Only.

* This specification is subject to change without notice.

Please contact Powertip or it's representative before designing your product based on this specification.

□ Approval For Specifications and Sample.

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History of Version

Date	Ver.	Description	Page	Design by
2007/9/6	0	Mass Production	-	LEO
2008/1/22	A	Add conductive double tape	LCM Drawing	Xuequn

Total: Page28

Contents

Note : For detailed information please refer to IC data sheet :

Primacy(TFT LCD)：Renesas--R61505U

I. SPECIFICATIONS

I.1 Features

Main LCD panel

Item	Standard Value
Display Type	240 *(R、G、B) * 320 Dots
LCD Type	a- si TFT，Positive，Transmissive
Screen size(inch)	3.2 (Diagonal)
Viewing Direction	9 O'clock
Color configuration	R.G.B. vertical stripe
Backlight	White LED B/L
Interface	8/16Bits data bus(i80 System Interface)
Other(controller/driver IC)	R61505U

I.2 Mechanical Specifications

Item	Standard Value	Unit
Outline Dimension	57.54 (W) * 79.2 (L) * 4.6 (H)	mm

LCD panel

Item	Standard Value	Unit
Active Area	48.6 (W) * 64.8 (L)	mm

Touch panel

Item	Standard Value	Unit
Viewing Area	51.2(W) * 71.85 (L)	mm
Active Area	49.6 (W) * 70.55 (L)	mm

Note : For detailed information please refer to LCM drawing

1.3 Absolute Maximum Ratings

Module

Item	Symbol	Condition	Min.	Max.	Unit
System Power Supply Voltage	VDD	-	-0.3	4.6	V
	VGH-VGL	-	-0.3	30	V
Input Voltage	V_I	-	-0.3	VDD +0.3	V
Operating Temperature	T_{OP}	Without T/P	-20	70	°C
Storage Temperature	T_{ST}	Without T/P	-30	80	°C
Storage Humidity	H_D	Ta < 40 °C	20	90	%RH

1.4 DC Electrical Characteristics

Module GND = 0V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	VDD	-	-	2.8	-	V
Input High Voltage	V_{IH}	-	0.8*VDD	-	VDD	V
Input Low Voltage	V_{IL}	-	-0.3	-	0.2*VDD	V
Output High Voltage	V_{OH}	-	0.8*VDD	-	-	V
Output Low Voltage	V_{OL}	-	0	-	0.2*VDD	V
Supply Current	IDD	VDD =2.8 V Pattern= full display	-	13.5	-	mA
		VDD =2.8 V Pattern= black *1		16.5	25	mA
Power Consumption	PW	-	-	38	-	mW

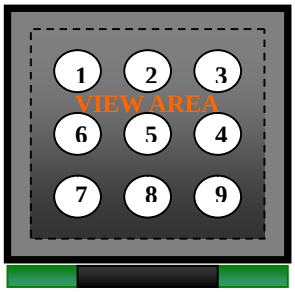
Note1:Maximum current display

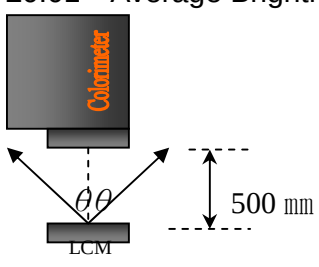
6.5 Optical Characteristics

TFT LCD panel Ta=25°C

Item		Symbol	Condition	Min.	Typ.	Max.	unit	
Response time	Rise	Tr +Tf	Ta = 25°C θX, θY = 0°	-	30	-	ms	Note2
	Fall							
Viewing angle	Top	θY+	CR ≥ 10	-	50	-	Deg.	Note4
	Bottom	θY-		-	50	-		
	Left	θX-		-	45	-		
	Right	θX+		-	50	-		
Contrast ratio		CR	Ta = 25°C θX , θY = 0°	200	250	-	-	Note3
Color of CIE Coordinate (With LCD & touch panel on)	White	X		0.25	0.30	0.35	-	Note1
		Y		0.27	0.32	0.37		
	Red	X		0.57	0.62	0.67		
		Y		0.31	0.36	0.41		
	Green	X		0.27	0.32	0.37		
		Y		0.55	0.60	0.65		
	Blue	X		0.10	0.15	0.20		
		Y		0.04	0.09	0.14		
Average Brightness Pattern=white display (With B/L & touch panel on)		IV	IF=100 mA	180	200	-	cd/m2	Note1
Uniformity (With B/L & touch panel on)		△B	IF=100 mA	80	-	-	%	Note1
NTSC			50				%	Note1

Note1:
1：△B=B(min) / B(max)
2：Measurement Condition for Optical Characteristics:
a：Environment: 25℃±5℃ / 60±20%R.H，no wind，dark room below 10 Lux at typical lamp current and typical operating frequency.
b：Measurement Distance: 500 ± 50 mm ，(θ= 0°)
c：Equipment: TOPCON BM-7 fast，(field 1°)，after 10 minutes operation.
d：The uncertainty of the C.I.E coordinate measurement ±0.01，Average Brightness ± 4%



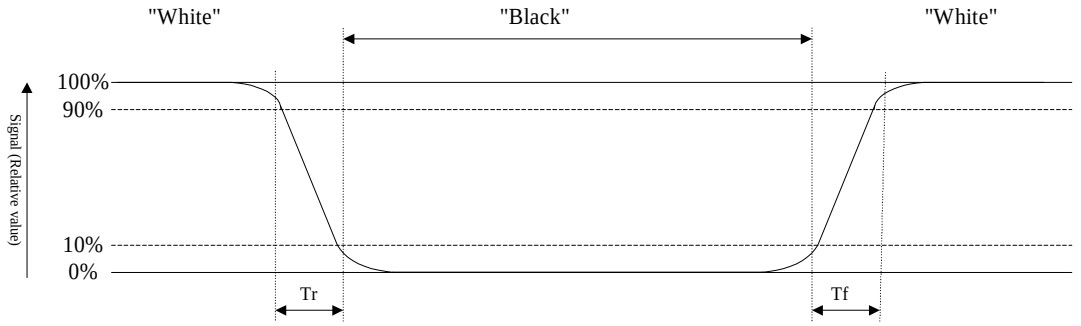


Colorimeter=BM-7 fast

Note2: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of Amplitudes.

Refer to figure as below:



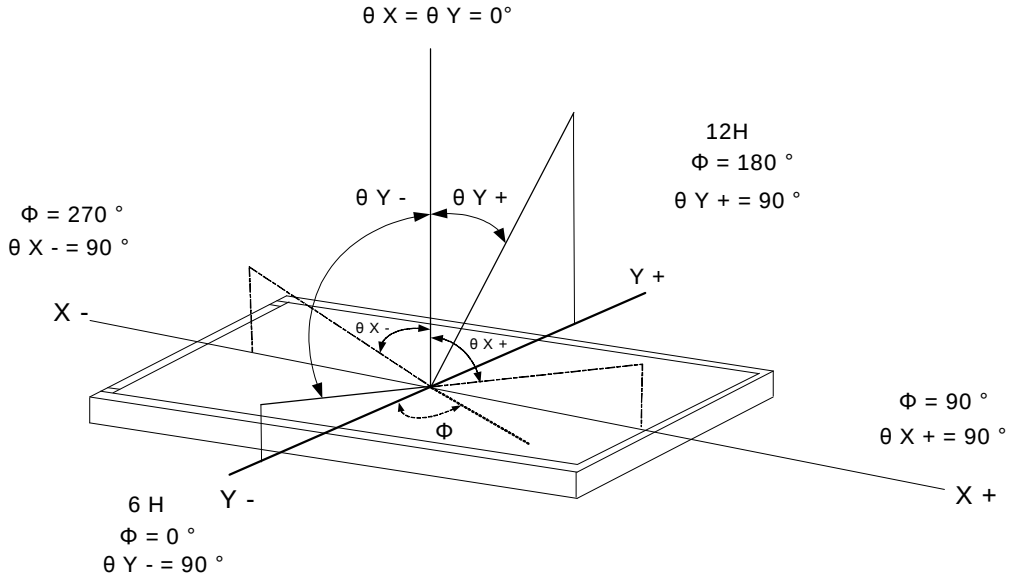
Note3: Definition of contrast ratio:

Contrast ratio is calculated with the following formula

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note4: Definition of viewing angle:

Refer to figure as below:



I.6 Backlight & LED Characteristics

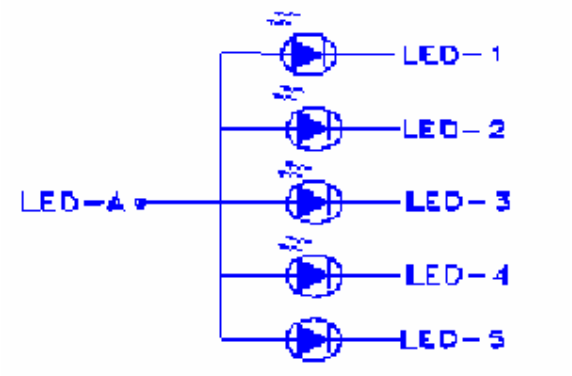
LCD Module with LED Backlight

Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Forward Voltage	VF	Ta =25℃	-	4	V
Forward Current	IF	Ta =25℃	-	150	mA
Reverse Voltage	VR	Ta =25℃	-	5	V
Power Dissipation	PD	Ta =25℃	-	600	mW

Electrical / Optical Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Voltage	VF	IF= 100mA	-	3.3	3.6	V
Average Brightness (Without LCD)	IV		3400	4000	-	cd/m^2
Color of CIE Coordinate (without LCD)	X		-	0.28	-	-
	Y		-	0.28	-	
Color	White					



1.7 Touch Panel Characteristics

General Standard Specification

Item	Specification
Input Method	Finger or Stylus pen.
ITO Glass(mm)	T=0.7 (mm).
ITO Film (μm)	T=180(μm).
Operating Temperature Range	-20℃~60℃,20~90%RH.
Storage Temperature Range	-40℃~40℃,< 90%RH, 41℃~70℃,< 60%RH.,
Surface Hardness	3H-pressure 500gf,45deg
Transparency	>82%.
Operation life	Tapping durability >1,000,000 times. Pen sliding durability >100,000 times.

Electrical Characteristic Specification

Item	Specification
Operating Voltage	DC 5V
Insulation Resistance	>20MΩ
Terminal Resistance	Film： 350-650 Ω
	Glass：120-430 Ω
Linearity	Less than 1.5%
Chattering Time	Less than 10 ms

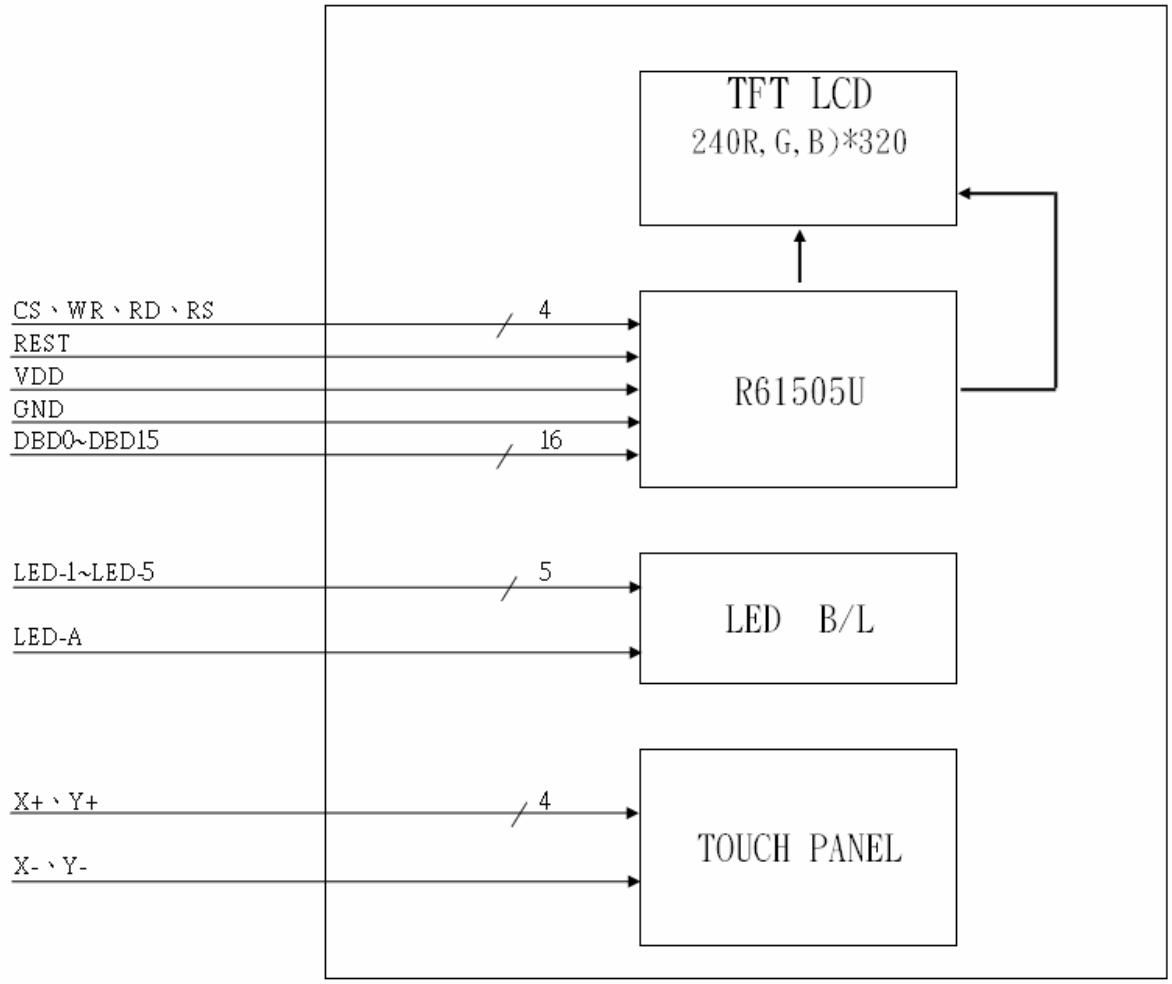
2. MODULE STRUCTURE

2.1 Counter Drawing

2.1.1 LCM Mechanical Diagram

* See Appendix

2.1.2 Block Diagram



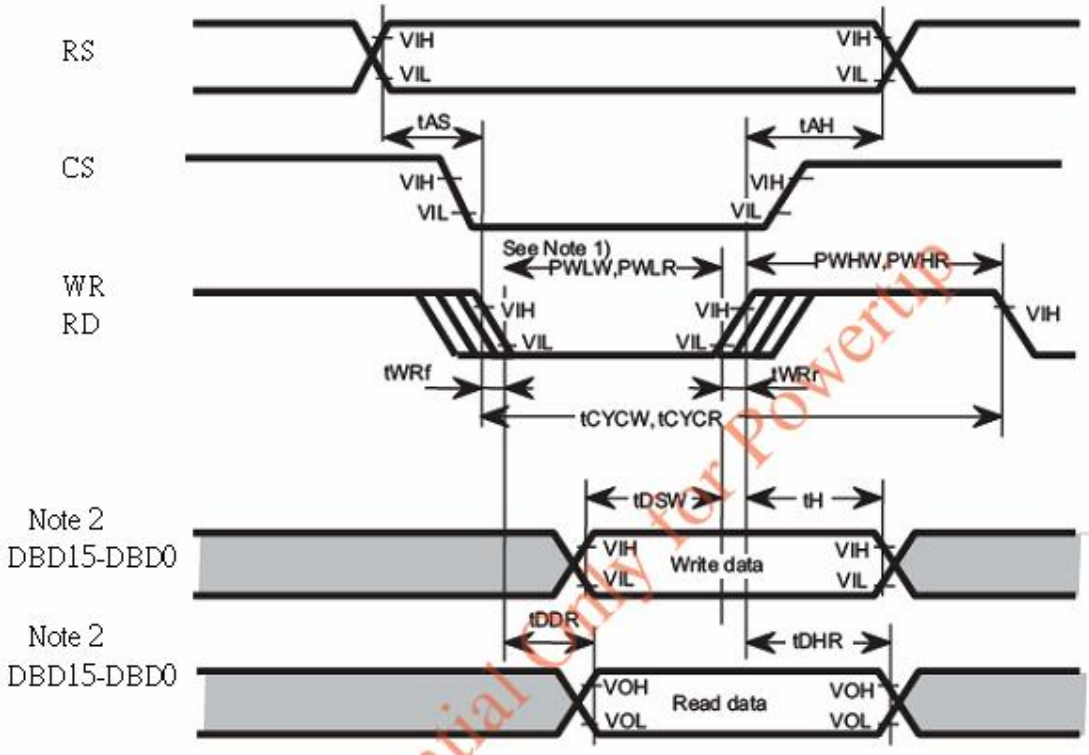
2.2 Interface Pin Description

Pin No	Symbol	Function
1	GND	System Ground.(0V)
2	VDD	Power supply(+2.8V)
3	VDD	Power supply(+2.8V)
4	CS	When CS=Low,Input/Output of Data/Command is enabled.
5	RS	Command / Display data selection High=Indicates that display data Low=Indicates that display data
6	WR	Connect WR signal. Active “L”.
7	RD	Connect RD signal. Active “L”.
8	REST	Reset input pin for TFT LCD. When RESET is “L”, initialization is executed.
9	DBD0	16Bit Data Bus
10	DBD1	
11	DBD2	
12	DBD3	
13	DBD4	
14	DBD5	
15	DBD6	
16	DBD7	
17	DBD8	
18	DBD9	
19	DBD10	
20	DBD11	
21	DBD12	
22	DBD13	
23	DBD14	
24	DBD15	

Pin No.	Symbol	Function
25	GND	System Ground.(0V)
26	Y-	Touch Panel output pin
27	X-	Touch Panel output pin
28	Y+	Touch Panel output pin
29	X+	Touch Panel output pin
30	LED-1	Backlight LED cathode input pin.
31	LED-2	Backlight LED cathode input pin.
32	LED-3	Backlight LED cathode input pin.
33	LED-4	Backlight LED cathode input pin.
34	LED-5	Backlight LED cathode input pin.
35	LED-A	Backlight LED anode input pin
36	LED-A	Backlight LED anode input pin
37	GND	System Ground.(0V)

2.3 Timing Characteristics

80-Sysyem Bus Operation



Note 1) PWLW and PWLR are defined by the overlap period when CS* is "Low" and WR* or RD* is "Low".
Note 2) Unused DB pins must be fixed at "IOVcc 1" or "IOGND 1".

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	Figure 93	125	-	-
	Read	tCYCR	ns	Figure 93	450	-	-
Write low-level pulse width		PWLW	ns	Figure 93	45	-	-
Read low-level pulse width		PWLR	ns	Figure 93	170	-	-
Write high-level pulse width		PWHW	ns	Figure 93	70	-	-
Read high-level pulse width		PWHR	ns	Figure 93	250	-	-
Write/Read rise/ fall time		tWRr, WRf	ns	Figure 93	-	-	25
Setup time	Write(RS~CS,WR)	tAS	ns	Figure 93	0	-	-
	Read (RS~CS,WR)		ns	Figure 93	10	-	-
Address Hold Time		tAH	ns	Figure 93	2	-	-
Write data setup time		tDSW	ns	Figure 93	25	-	-
Write data hold time		tH	ns	Figure 93	10	-	-
Read data delay time		tDDR	ns	Figure 93	-	-	150
Read data hold time		tDHR	ns	Figure 93	5	-	-

2.4 Instruction Table

LCD-IC：R61505U

dex	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
—	Index	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0H	Device Code Read	0	0	0	1	0	1	0	1	0	0	0	0	0	1	0	1
1H	Driver Output Control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	0
2H	LCD Driver Waveform Control	0	0	0	0	0	1 (1)	BC0 (0)	EOR (0)	0	0	0	0	0	0	0	NW0 (0)
3H	Entry mode	TRIREG (0)	DFM (0)	0	BGR (0)	0	0	HWM (0)	0	ORG (0)	0	ID1 (1)	ID0 (1)	AM (0)	0	0	0
4H	Resize control	0	0	0	0	0	0	RCV[1] (0)	RCV[0] (0)	0	0	RCH[1] (0)	RCH[0] (0)	0	0	RSZ[1] (0)	RSZ[0] (0)
H-06H	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
7H	Display Control 1	0	0	PTDE[1] (0)	PTDE[0] (0)	0	0	0	BASEE (0)	0	VON (0)	GON (0)	DTE (0)	COL (0)	0	D[1] (0)	D[0] (0)
8H	Display Control 2	0	0	0	0	FP[3] (1)	FP[2] (0)	FP[11] (0)	FP[0] (0)	0	0	0	0	BP[3] (1)	BP[2] (0)	BP[1] (0)	BP[0] (0)
9H	Display Control 3	0	0	0	0	0	PTS[2] (0)	PTS[1] (0)	PTS[0] (0)	0	0	PTG[1] (0)	PTG[0] (0)	ISC[3] (0)	ISC[2] (0)	ISC[1] (0)	ISC[0] (0)
AH	Display Control 4	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE(0)	FMI[2] (0)	FMI[1] (0)	FMI[0] (0)
BH	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
CH	External Displaly Interface Control 1	0	ENC[2] (0)	ENC[1] (0)	ENC[0] (0)	0	0	0	RM (0)	0	0	DM[1] (0)	DM[0] (0)	0	0	RIM[1] (0)	RIM[0] (0)
DH	Frame Marker Control	0	0	0	0	0	0	0	FMP[8] (0)	FMP[7] (0)	FMP[6] (0)	FMP[5] (0)	FMP[4] (0)	FMP[3] (0)	FMP[2] (0)	FMP[1] (0)	FMP[0] (0)
EH	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
FH	External Displaly Interface Control 2	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)
0H	Power Control 1	0	0	0	SAP (0)	BT[3] (0)	BT[2] (0)	BT[1] (0)	BT[0] (0)	APE (0)	0	AP[1] (0)	AP[0] (0)	0	DSTB (0)	SLP (0)	0
1H	Power Control 2	0	0	0	0	0	DC1[2] (1)	DC1[1] (1)	DC1[0] (0)	0	DC0[2] (1)	DC0[1] (1)	DC0[0] (0)	0	VC[2] (0)	VC[1] (0)	VC[0] (0)
2H	Power Control 3	0	0	0	0	0	0	0	VCMR[0] (0)	VREG1R (0)	0	PSON (0)	PON (0)	VRH[3] (0)	VRH[2] (0)	VRH[1] (0)	VRH[0] (0)
3H	Power Control 4	0	0	0	VDV[4] (0)	VDV[3] (0)	VDV[2] (0)	VDV[1] (0)	VDV[0] (0)	0	0	0	0	0	0	0	0
H-16H	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
7H	Power Control 5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE (0)
H-1FH	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
0H	RAM Address Set(Horizontal)	0	0	0	0	0	0	0	0	AD[7] (0)	AD[6] (0)	AD[5] (0)	AD[4] (0)	AD[3] (0)	AD[2] (0)	AD[1] (0)	AD[0] (0)
1H	RAM Address Set(Vertical)	0	0	0	0	0	0	0	AD[16] (0)	AD[15] (0)	AD[14] (0)	AD[13] (0)	AD[12] (0)	AD[11] (0)	AD[10] (0)	AD[9] (0)	AD[8] (0)

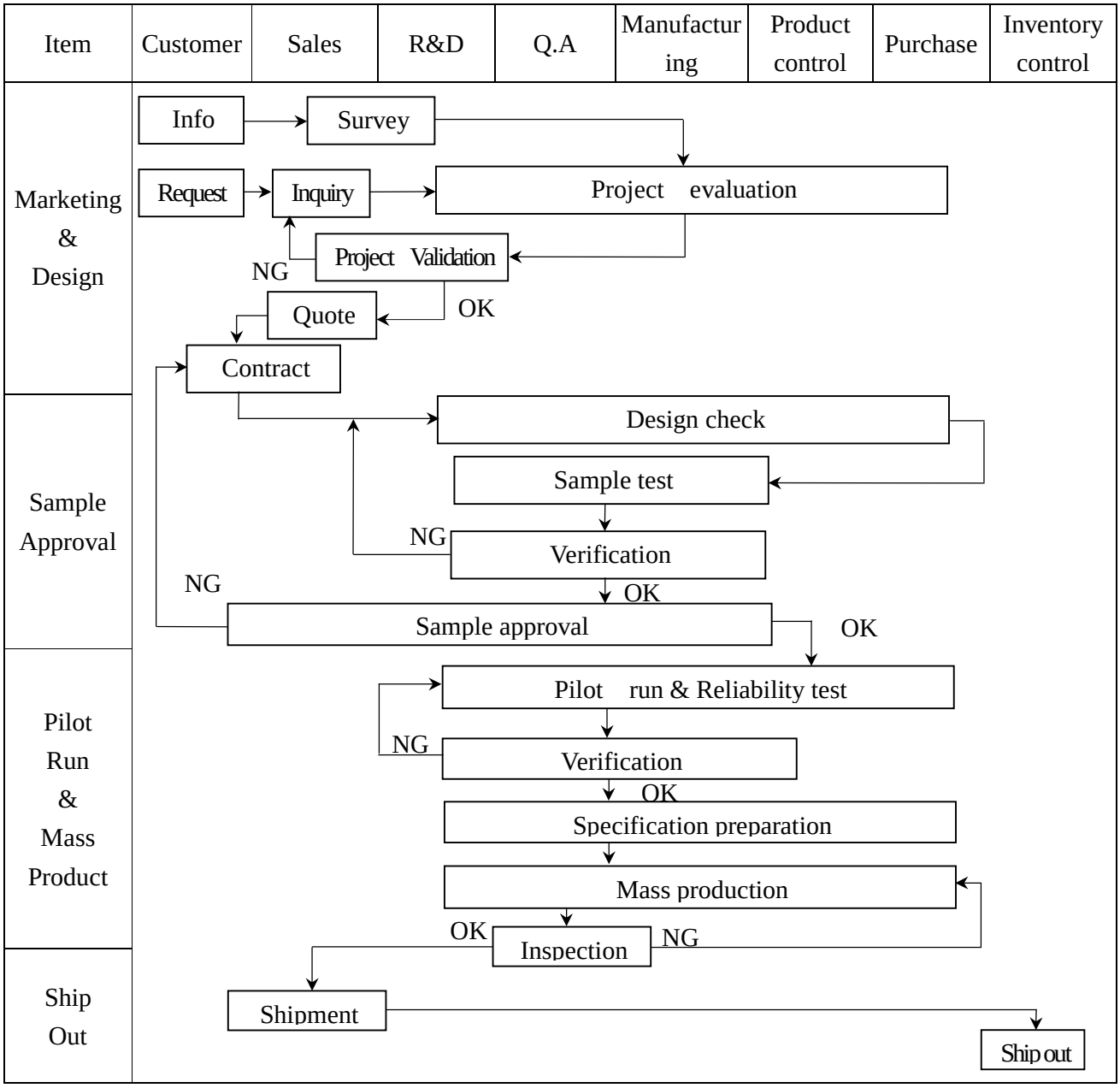
2H	Write Data to/Read Data from GRAM	RAM write data(WD17-0)/RAM read data(RD17-0) bits are allocated to different data bus according to the format of selected interface															
dex	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
H-27H	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
8H	NVM Read Data 1	0	0	0	0	0	0	0	0	0	0	0	0	UID[3] (0)	UID[2] (0)	UID[1] (0)	UID[0] (0)
9H	NVM Read Data 2	0	0	0	0	0	0	0	0	0	0	0	VCM1[4] (0)	VCM1[3] (0)	VCM1[2] (0)	VCM1[1] (0)	VCM1[0] (0)
AH	NVM Read Data 3	0	0	0	0	0	0	0	0	VCMSEL (0)	0	0	VCM2[4] (0)	VCM2[3] (0)	VCM2[2] (0)	VCM2[1] (0)	VCM2[0] (0)
H-2FH	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
0H	γ Control 1	0	0	0	0	0	P0KP1[2] (0)	P0KP1[1] (0)	P0KP1[0] (0)	0	0	0	0	0	P0KP0[2] (0)	P0KP0[1] (0)	P0KP0[0] (0)
1H	γ Control 2	0	0	0	0	0	P0KP3[2] (0)	P0KP3[1] (0)	P0KP3[0] (0)	0	0	0	0	0	P0KP2[2] (0)	P0KP2[1] (0)	P0KP2[0] (0)
2H	γ Control 3	0	0	0	0	0	P0KP5[2] (0)	P0KP5[1] (0)	P0KP5[0] (0)	0	0	0	0	0	P0KP4[2] (0)	P0KP4[1] (0)	P0KP4[0] (0)
3H	γ Control 4	0	0	0	0	0	0	P0FP1[1] (0)	P0FP1[0] (0)	0	0	0	0	0	0	P0FP0[1] (0)	P0FP0[0] (0)
4H	γ Control 5	0	0	0	0	0	0	P0FP3[1] (0)	P0FP3[0] (0)	0	0	0	0	0	0	P0FP2[1] (0)	P0FP2[0] (0)
5H	γ Control 6	0	0	0	0	0	P0RP1[2] (0)	P0RP1[1] (0)	P0RP1[0] (0)	0	0	0	0	0	P0RP0[2] (0)	P0RP0[1] (0)	P0RP0[0] (0)
6H	γ Control 7	0	0	0	V0RP1[4](0)	V0RP1[3](0)	V0RP1[2](0)	V0RP1[1](0)	V0RP1[0] (0)	0	0	0	V0RP0[4] (0)	V0RP0[3] (0)	V0RP0[2](0)	V0RP0[1](0)	V0RP0[0](0)
7H	γ Control 8	0	0	0	0	0	P0KN1[2](0)	P0KN1[1](0)	P0KN1[0] (0)	0	0	0	0	0	P0KN0[2](0)	P0KN0[1](0)	P0KN0[0](0)
8H	γ Control 9	0	0	0	0	0	P0KN3[2](0)	P0KN3[1](0)	P0KN3[0] (0)	0	0	0	0	0	P0KN2[2](0)	P0KN2[1](0)	P0KN2[0](0)
9H	γ Control 10	0	0	0	0	0	P0KN5[2](0)	P0KN5[1](0)	P0KN5[0] (0)	0	0	0	0	0	P0KN4[2](0)	P0KN4[1](0)	P0KN4[0](0)
AH	γ Control 11	0	0	0	0	0	0	P0FN1[1] (0)	P0FN1[0] (0)	0	0	0	0	0	0	P0FN0[1] (0)	P0FN0[0] (0)
BH	γ Control 12	0	0	0	0	0	0	P0FN3[1] (0)	P0FN3[0] (0)	0	0	0	0	0	0	P0FN2[1](0)	P0FN2[0] (0)
CH	γ Control 13	0	0	0	0	0	P0RN1[2](0)	P0RN1[1](0)	P0RN1[0] (0)	0	0	0	0	0	P0RN0[2](0)	P0RN0[1](0)	P0RN0[0](0)
DH	γ Control 14	0	0	0	V0RN1[4](0)	V0RN1[3](0)	V0RN1[2](0)	V0RN1[1](0)	V0RN1[0](0)	0	0	0	V0RN0[4](0)	V0RN0[3] (0)	V0RN0[2] (0)	V0RN0[1](0)	V0RN0[0](0)
H-3FH	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
0H	Window Horizontal RAM Address(Start Address)	0	0	0	0	0	0	0	0	HAS[7] (0)	HAS[6] (0)	HAS[5] (0)	HAS[4] (0)	HAS[3] (0)	HAS[2] (0)	HAS[1] (0)	HAS[0] (0)
1H	Window Horizontal RAM Address(End Address)	0	0	0	0	0	0	0	0	HEA[7] (1)	HEA[6] (1)	HEA[5] (1)	HEA[4] (0)	HEA[3] (1)	HEA[2] (1)	HEA[1] (1)	HEA[0] (1)
2H	Window Vertical RAM Address(Start Address)	0	0	0	0	0	0	0	VSA[8] (0)	VSA[7] (0)	VSA[6] (0)	VSA[5] (0)	VSA[4] (0)	VSA[3] (0)	VSA[2] (0)	VSA[1] (0)	VSA[0] (0)
3H	Window Vertical RAM Address(End Address)	0	0	0	0	0	0	0	VEA[8] (1)	VEA[7] (0)	VEA[6] (0)	VEA[5] (1)	VEA[4] (1)	VEA[3] (1)	VEA[2] (1)	VEA[1] (1)	VEA[0] (1)

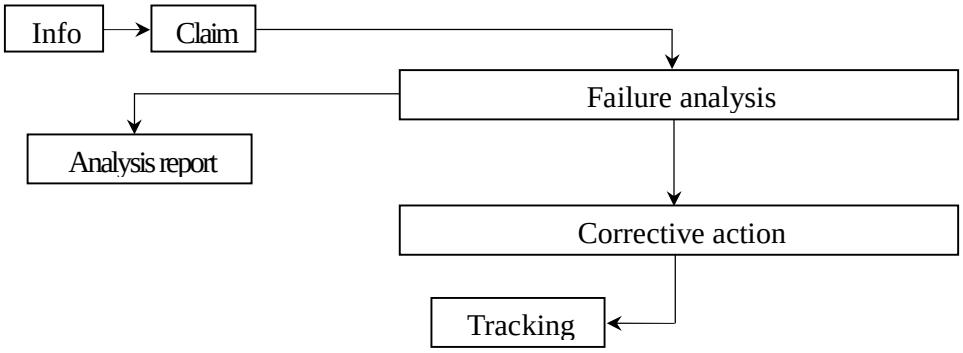
H-5FH	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
dex	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0H	Driver Output Control	GS(0)	0	NL[5] (0)	NL[4] (0)	NL[3] (0)	NL[2] (0)	NL[1] (0)	NL[0] (0)	0	0	SCN[5] (0)	SCN[4] (0)	SCN[3] (0)	SCN[2] (0)	SCN[1] (0)	SCN[0] (0)
1H	Base Image Display Control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)
H-69H	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
AH	Vertical Scroll Control	0	0	0	0	0	0	0	VL[8] (0)	VL[7] (0)	VL[6] (0)	VL[5] (0)	VL[4] (0)	VL[3] (0)	VL[2] (0)	VL[1] (0)	VL[0] (0)
H-6FH	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
0H	Partial Image 1 Display Position	0	0	0	0	0	0	0	PTDP0[8] (0)	PTDP0[7] (0)	PTDP0[6] (0)	PTDP0[5] (0)	PTDP0[4] (0)	PTDP0[3] (0)	PTDP0[2] (0)	PTDP0[1] (0)	PTDP0[0] (0)
1H	Partial Image 1 RAM Address(Start Line Address)	0	0	0	0	0	0	0	PTSA0[8] (0)	PTSA0[7] (0)	PTSA0[6] (0)	PTSA0[5] (0)	PTSA0[4] (0)	PTSA0[3] (0)	PTSA0[2] (0)	PTSA0[1] (0)	PTSA0[0] (0)
2H	Partial Image 1 RAM Address(End Line Address)	0	0	0	0	0	0	0	PTEA0[8](0)	PTEA0[7](0)	PTEA0[6](0)	PTEA0[5](0)	PTEA0[4](0)	PTEA0[3](0)	PTEA0[2](0)	PTEA0[1](0)	PTEA0[0](0)
3H	Partial Image 2 Display Position	0	0	0	0	0	0	0	PTDP1[8] (0)	PTDP1[7] (0)	PTDP1[6] (0)	PTDP1[5] (0)	PTDP1[4] (0)	PTDP1[3] (0)	PTDP1[2] (0)	PTDP1[1] (0)	PTDP1[0] (0)
4H	Partial Image 2 RAM Address(Start Line Address)	0	0	0	0	0	0	0	PTSA1[8] (0)	PTSA1[7] (0)	PTSA1[6] (0)	PTSA1[5] (0)	PTSA1[4] (0)	PTSA1[3] (0)	PTSA1[2] (0)	PTSA1[1] (0)	PTSA1[0] (0)
5H	Partial Image 2 RAM Address(End Line Address)	0	0	0	0	0	0	0	PTEA1[8](0)	PTEA1[7] (0)	PTEA1[6](0)	PTEA1[5](0)	PTEA1[4](0)	PTEA1[3](0)	PTEA1[2](0)	PTEA1[1](0)	PTEA1[0](0)
H-8FH	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
0H	Panel Interface Control 1	0	0	0	0	0	0	DIVI[1] (0)	DIVI[1] (0)	0	0	0	RTNI[4] (1)	RTNI[3] (0)	RTNI[2] (0)	RTNI[1] (0)	RTNI[0] (0)
1H	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
2H	Panel Interface Control 2	0	0	0	0	0	NOWI[2] (0)	NOWI[1] (0)	NOWI[0] (0)	0	0	0	0	0	0	0	0
3H	Panel Interface Control 3	0	0	0	0	0	0	VEQWI[1](0)	VEQWI[0](0)	0	0	0	0	0	MCPI[2] (0)	MCPI[1] (0)	MCPI[0] (0)
4H	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
5H	Panel Interface Control 4	0	0	0	0	0	0	DIVE[1] (1)	DIVE[0] (0)	0	0	RTNE[5] (0)	RTNE[4] (1)	RTNE[3] (1)	RTNE[2] (1)	RTNE[1] (1)	RTNE[0] (0)
6H	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
7H	Panel Interface Control 5	0	0	0	0	NOWE[3] (0)	NOWE[2] (0)	NOWE[1] (0)	NOWE[0] (0)	0	0	0	0	0	0	0	0

8H	Panel Interface Control 6	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE[2] (0)	MCPE[1] (0)	MCPE[0] (0)
dex	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
H-9F H	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
.0H	NVM Access Control 1	0	0	0	0	0	0	0	0	TE (0)	0	EOP[1] (0)	EOP[0] (0)	0	0	EAD[1] (0)	EAD[0] (0)
.1H	NVM Access Control 2	0	0	0	0	0	0	0	0	ED7 (0)	0	0	ED4 (0)	ED3 (0)	ED2 (0)	ED1 (0)	ED0 (0)
H-A3 H	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
.4H	Calibration Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB (0)
H-A H	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
H-F* H	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited

3. QUALITY ASSURANCE SYSTEM

3.1 Quality Assurance Flow Chart



Item	Customer	Sales	R&D	Q.A	Manufacturing	Product control	Purchase	Inventory control
Sales Service								
Q.A Activity	1. ISO 9001 Maintenance Activities 2. Process improvement proposal 3. Equipment calibration 4. Education And Training Activities 5. Standardization Management							

3.2 Inspection Specification

◆Scope ：The document shall be applied to TFT-LCD Module for less than 3.5″ (Ver.02).

◆Inspection Standard：MIL-STD-105E Table Normal Inspection Single Sampling Level Ⅱ.

◆Equipment：Gauge、MIL-STD、Powertip Tester、Sample

◆Defect Level：Major Defect AQL： 0.4 ； Minor Defect AQL： 1.5

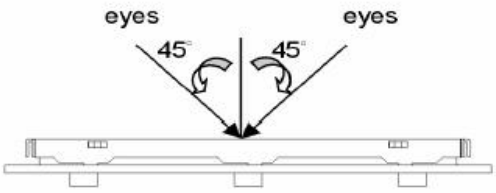
◆OUT Going Defect Level：Sampling.

◆Standard of the product appearance test：

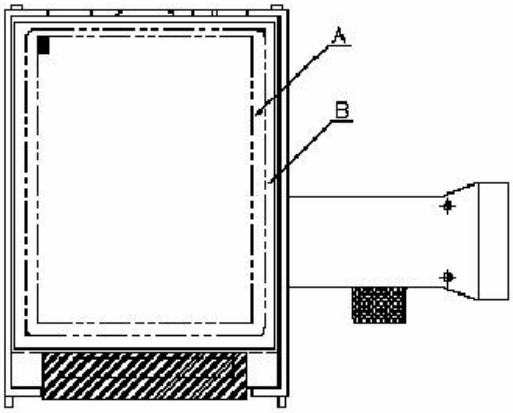
a. Manner of appearance test：

(1). The test best be under 20W×2 fluorescent light，and distance of view must be at 30 cm.

(2). The test direction is base on about around 45° of vertical line.



(3). Definition of area.



A area : viewing area

B area : Outside of viewing area

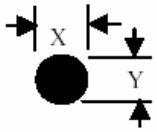
(4). Standard of inspection： (Unit：mm)

◆Specification For TFT-LCD Module Less Than 3.5″： (Ver.02)

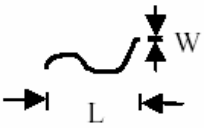
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>Level</th></tr>
<tr><td rowspan="3">01</td><td rowspan="3">Product condition</td><td>1.1The part number is inconsistent with work order of production.</td><td>Major</td></tr>
<tr><td>1.2 Mixed product types.</td><td>Major</td></tr>
<tr><td>1.3 Assembled in inverse direction.</td><td>Major</td></tr>
<tr><td>02</td><td>Quantity</td><td>2.1The quantity is inconsistent with work order of production.</td><td>Major</td></tr>
<tr><td>03</td><td>Outline dimension</td><td>3.1 Product dimension and structure must conform to structure diagram.</td><td>Major</td></tr>
<tr><td rowspan="5">04</td><td rowspan="5">Electrical Testing</td><td>4.1 Missing line character and icon.</td><td>Major</td></tr>
<tr><td>4.2 No function or no display.</td><td>Major</td></tr>
<tr><td>4.3 Display malfunction.</td><td>Major</td></tr>
<tr><td>4.4 LCD viewing angle defect.</td><td>Major</td></tr>
<tr><td>4.5 Current consumption exceeds product specifications.</td><td>Major</td></tr>
<tr><td>05</td><td>Dot defect
(Bright dot、Dark dot)
On -display</td><td>
<table>
<tr><th colspan="2">Item</th><th>Acceptance (Q'ty)</th></tr>
<tr><td rowspan="4">Dot Defect</td><td>Bright Dot</td><td>≦ 2</td></tr>
<tr><td>Dark Dot</td><td>≦ 3</td></tr>
<tr><td>Joint Dot</td><td>≦ 2</td></tr>
<tr><td>Total</td><td>≦ 3</td></tr>
</table>
5.1 Inspection pattern：full white , full black , Red , Green and blue screens.
5.2 It is defined as dot defect if defect area ＞1/2 dot.
5.3 The distance between two dot defect ≧5 mm.
</td><td>Minor</td></tr>
</table>

◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.02)

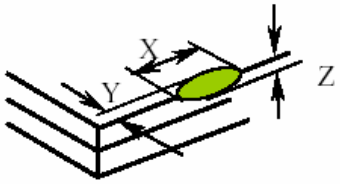
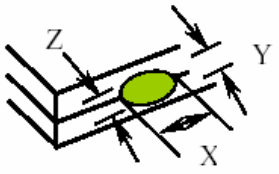
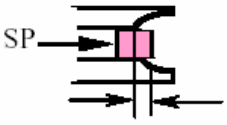
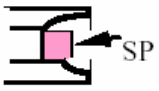
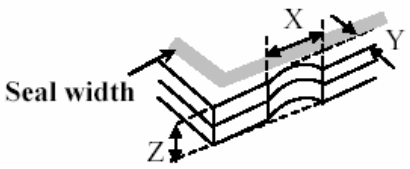
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>Level</th></tr>
<tr><td>06</td><td>Black or white dot、scratch、contamination

Round type
 

Φ=(x+y) / 2

Line type
 
</td><td>6.1 Round type (Non-display or display) :
<table><tr><th>Dimension (diameter : Φ)</th><th>Acceptance (Q'ty)</th></tr><tr><td>Φ ≦ 0.15</td><td>Ignore</td></tr><tr><td>0.15 < Φ ≦ 0.20</td><td>2</td></tr><tr><td>0.20 < Φ ≦ 0.30</td><td>2</td></tr><tr><td>Φ > 0.30</td><td>0</td></tr><tr><td>Total</td><td>3</td></tr></table>
6.2 Line type(Non-display or display) :
<table><tr><th>Length (L)</th><th>Width (W)</th><th>Acceptance (Q'ty)</th></tr><tr><td>---</td><td>W ≦ 0.03</td><td>Ignore</td></tr><tr><td>L ≦5.0</td><td>0.03 < W ≦ 0.05</td><td>3</td></tr><tr><td>---</td><td>W >0.05</td><td>As round type</td></tr><tr><td colspan="2">Total</td><td>3</td></tr></table></td><td>Minor</td></tr>
<tr><td>07</td><td>Polarizer Bubble</td><td><table><tr><th>Dimension (diameter : Φ)</th><th>Acceptance (Q'ty)</th></tr><tr><td>Φ ≦ 0.20</td><td>Ignore</td></tr><tr><td>0.20 < Φ ≦ 0.50</td><td>3</td></tr><tr><td>Φ > 0.50</td><td>0</td></tr><tr><td>Total</td><td>3</td></tr></table></td><td>Minor</td></tr>
</table>

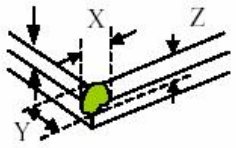
◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.02)

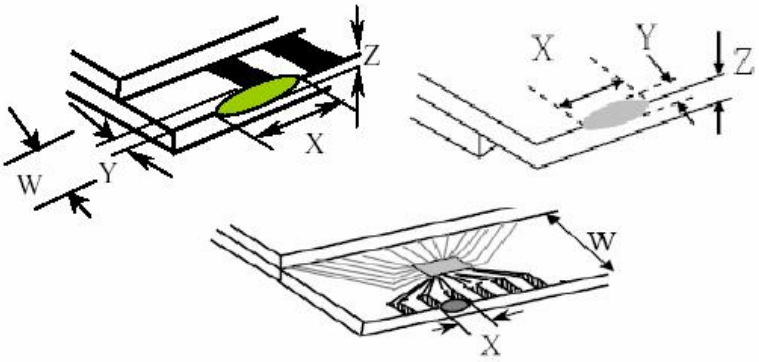
NO	Item	Criterion	Level
08	The crack of glass	Symbols : X : The length of crack Y : The width of crack. Z : The thickness of crack W : terminal length t : The thickness of glass a : LCD side length 8.1 General glass chip : 8.1.1 Chip on panel surface and crack between panels:    【OK】  【NG】  X | Y | Z ≦ a | Crack can't enter viewing area | ≦1/2 t ≦ a | Crack can't exceed the half of SP width. | 1/2 t < Z ≦2 t	Minor

◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.02)

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>Level</th></tr>
<tr><td>08</td><td>The crack of glass</td><td>
Symbols :

X : The length of crack　　Y : The width of crack.
Z : The thickness of crack　　W : terminal length
t : The thickness of glass　　a : LCD side length

8.1.2 Corner crack :


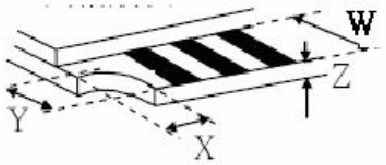
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≦1/5 a</td><td>Crack can't enter viewing area</td><td>Z ≦ 1/2 t</td></tr>
<tr><td>≦1/5 a</td><td>Crack can't exceed the half of SP width.</td><td>1/2 t < Z ≦ 2 t</td></tr>
</table>
8.2 Protrusion over terminal :
8.2.1 Chip on electrode pad :


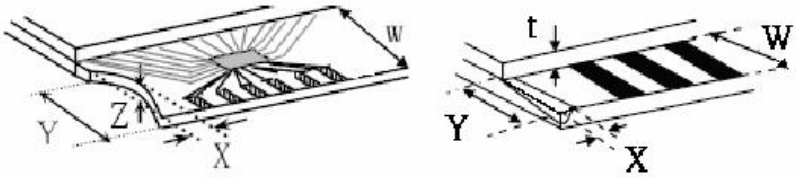
<table>
<tr><th></th><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>Front</td><td>≦ a</td><td>≦ 1/2 W</td><td>≦ t</td></tr>
<tr><td>Back</td><td>≦ a</td><td>≦ W</td><td>≦ 1/2 t</td></tr>
</table>
</td><td>Minor</td></tr>
</table>

◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.02)

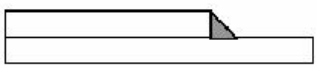
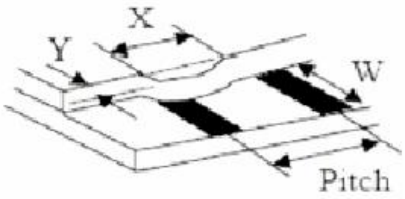
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>Level</th></tr>
<tr><td>08</td><td>The crack of glass</td><td>
Symbols :

X : The length of crack　　Y : The width of crack.
Z : The thickness of crack　　W : terminal length
t : The thickness of glass　　a : LCD side length

8.2.2 Non-conductive portion :




<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≦ 1/3 a</td><td>≦W</td><td>≦t</td></tr>
</table>
⊙ If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.

8.2.3 Glass remain :



<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≦ a</td><td>≦ 1/3 W</td><td>≦t</td></tr>
</table>
</td><td>Minor</td></tr>
</table>

◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.02)

NO	Item	Criterion	Level
09	Backlight elements	9.1 Backlight can't work normally.	Major
		9.2 Backlight doesn't light or color is wrong.	Major
		9.3 Illumination source flickers when lit.	Major
10	General appearance	10.1 Pin type、quantity、dimension must match type in structure diagram.	Major
		10.2 No short circuits in components on PCB or FPC .	Major
		10.3 Parts on PCB or FPC must be the same as on the production characteristic chart .There should be no wrong parts , missing parts or excess parts.	Major
		10.4 Product packaging must the same as specified on packaging specification sheet.	Minor
		10.5 The folding and peeled off in polarizer are not acceptable.	Minor
		10.6 The PCB or FPC between B/L assembled distance(PCB or FPC) is ≦1.5 mm.	Minor

4. RELIABILITY TEST

4.1 Reliability Test Condition

Ver.02

NO.	TEST ITEM	TEST CONDITION
1	High Temperature Storage Test	Keep in +80 ±2℃ 96 hrs Surrounding temperature, then storage at normal condition 4hrs.
2	Low Temperature Storage Test	Keep in -30 ±2℃ 96 hrs Surrounding temperature, then storage at normal condition 4hrs.
3	High Temperature / High Humidity Storage Test	Keep in +60℃ / 90% R.H duration for 96 hrs Surrounding temperature, then storage at normal condition 4hrs. (Excluding the polarizer)
4	ESD Test	Air Discharge: Apply 2 KV with 5 times Discharge for each polarity +/- Contact Discharge: Apply 250 V with 5 times discharge for each polarity +/- 1. Temperature ambiance : 15℃～35℃ 2. Humidity relative : 30%～60% 3. Energy Storage Capacitance(Cs+Cd) : 150pF±10% 4. Discharge Resistance(Rd) : 330Ω±10% 5. Discharge, mode of operation : Single Discharge (time between successive discharges at least 1 sec) (Tolerance if the output voltage indication : ±5%)
5	Temperature Cycling Storage Test	-20℃ → +25℃ → +70℃ → +25℃ (30mins) (5mins) (30mins) (5mins) 10 Cycle Surrounding temperature, then storage at normal condition 4hrs.
6	Vibration Test (Packaged)	1. Sine wave 10～55 Hz frequency (1 min) 2. The amplitude of vibration :1.5 mm 3. Each direction (X、Y、Z) duration for 2 Hrs
7	Drop Test (Packaged)	Packing Weight (Kg) / Drop Height (cm): 0 ~ 45.4 — 122 45.4 ~ 90.8 — 76 90.8 ~ 454 — 61 Over 454 — 46 Drop direction :※1 corner / 3 edges / 6 sides each 1times

5. PRECAUTION RELATING PRODUCT HANDLING

5.1 SAFETY

5.1.1 If the LCD panel breaks , be careful not to get the liquid crystal to touch your skin.

5.1.2 If the liquid crystal touches your skin or clothes , please wash it off immediately by using soap and water.

5.2 HANDLING

5.2.1 Avoid any strong mechanical shock which can break the glass.

5.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module , be sure to ground your body and any electrical equipment you may be using.

5.2.3 Do not remove the panel or frame from the module.

5.2.4 The polarizing plate of the display is very fragile. So , please handle it very carefully, do not touch , push or rub the exposed polarizing with anything harder than an HB pencil lead (glass , tweezers , etc.)

5.2.5 Do not wipe the polarizing plate with a dry cloth , as it may easily scratch the surface of plate.

5.2.6 Do not touch the display area with bare hands , this will stain the display area.

5.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.

5.2.8 To control temperature and time of soldering is 320 ± 10°C and 3-5 sec.

5.2.9 To avoid liquid (include organic solvent) stained on LCM

5.3 STORAGE

5.3.1 Store the panel or module in a dark place where the temperature is 25°C ± 5°C and the humidity is below 65% RH.

5.3.2 Do not place the module near organics solvents or corrosive gases.

5.3.3 Do not crush , shake , or jolt the module.

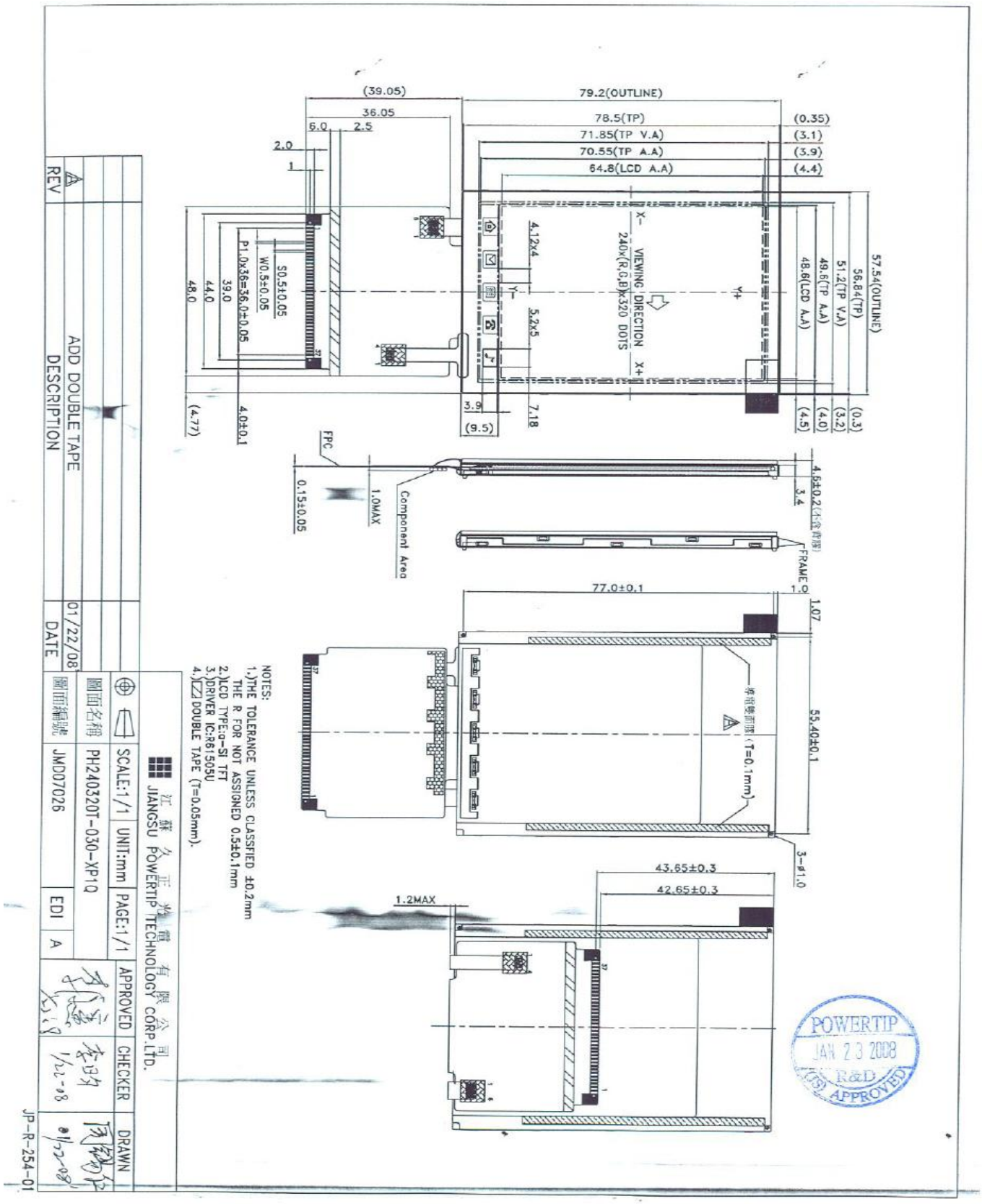
5.4 TERMS OF WARRANTY

5.4.1 Applicable warrant period

The period is within thirteen months since the date of shipping out under normal using and storage conditions.

5.4.2 Unaccepted responsibility

This product has been manufactured to your company's specification as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in nuclear power control equipment, aerospace equipment , fire and security systems or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required.


(39.05)
79.2(OUTLINE)
36.05
78.5(TP)
(0.35)
6.0
2.5
71.85(TP V.A)
(3.1)
2.0
70.55(TP A.A)
(3.9)
1
64.8(LCD A.A)
(4.4)
57.54(OUTLINE)
56.84(TP)
51.2(TP V.A)
49.6(TP A.A)
48.6(LCD A.A)
(0.3)
(3.2)
(4.0)
(4.5)
4.12x4
5.2x5
240x(R,G,B)x320 DOTS
VIEWING DIRECTION
X-
X+
Y-
Y+
P1.0x36=36.0±0.05
W0.5±0.05
S0.5±0.05
39.0
44.0
48.0
(4.77)
4.0±0.1
3.9
(9.5)
7.18
FPC
0.15±0.05
1.0MAX
Component Area
4.6±0.2(不含背膠)
3.4
FRAME
77.0±0.1
1.0
1.07
55.40±0.1
停留雙面膠(T=0.1mm)
3-φ1.0
43.65±0.3
42.65±0.3
1.2MAX
NOTES:
1.)THE TOLERANCE UNLESS CLASSFIED ±0.2mm
THE R FOR NOT ASSIGNED 0.5±0.1mm
2.)LCD TYPE:a-Si TFT
3.)DRIVER IC:R61505U
4.)ZZ DOUBLE TAPE (T=0.05mm).
REV
DESCRIPTION
DATE
ADD DOUBLE TAPE
01/22/08
江蘇久正光電有限公司
JIANGSU POWERTIP TECHNOLOGY CORP.LTD.
SCALE:1/1
UNIT:mm
PAGE:1/1
圖面名稱
PH240320T-030-XP1Q
圖面編號
JMD07026
EDI
A
APPROVED
CHECKER
DRAWN
JP-R-254-01
POWERTIP
JAN 23 2008
R&D
APPROVED

LCM Model	PH240320T-030-XP1Q
Drawing NO.	ASS-5-872

LCM包裝規格書
LCM Packaging Specifications

Approve	Check	Contact
DATE	初版	版次Ver
09.06.07	09.06.07	0

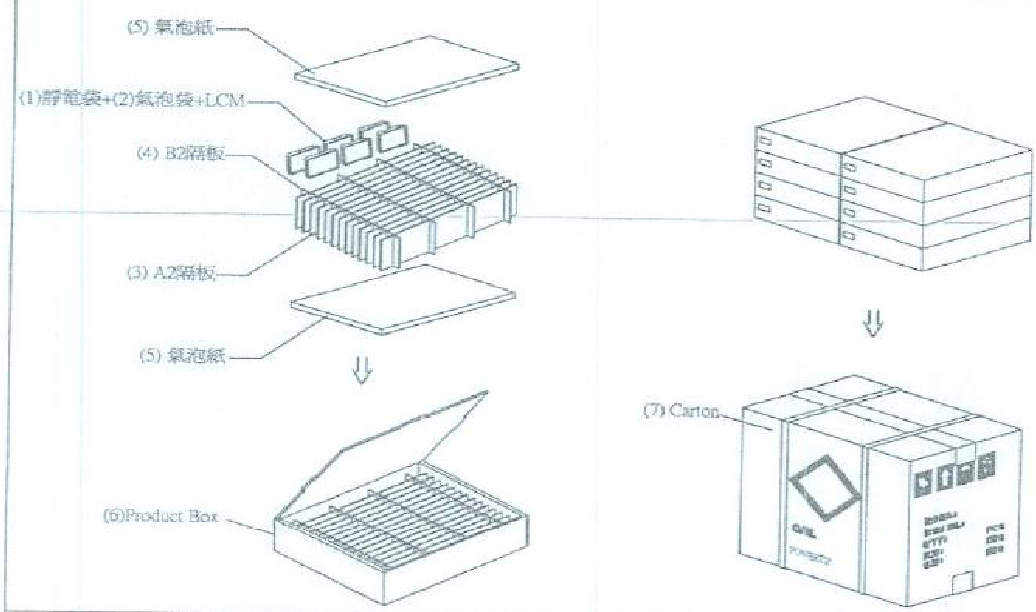
1.包裝材料規格表 (Packaging Material) : (per carton)

No.	Item	Model	Dimensions (mm)	Quantity
1	成品 (LCM)	PH240320T-030-XP1Q	57.54X79.2	288
2	靜電袋(1)Antistatic Bag	BAG150120ARABA	150 X 120	288
3	氣泡袋(2)	BAG100080BWABA	80 X(100+30)	288
4	A2隔板(3)A2 Partition	BX29300070BMBA	293 X 70 X 3	88
5	B2隔板(4)B2 Partition	BX24500070BLBA	245 X 70 X 3	32
6	氣泡紙(5)Bubble Sheet	BAG280240BWABA	280 X 240	16
7	C2內盒(6)Product Box	BX31025580AABA	310 X 255 X 86	8
8	外紙箱(7)Carton	BX52732536CCBA	527 X 325 X 360	1
9				

2.單箱數量規格表 (Packaging Specifications and Quantity) :

(1)Quantity Of Spacer : A2隔板 X 11 , B2隔板 X 4

(2)Total LCM quantity in carton : quantity per box 36 x no of boxes 8 = 288



特記事項(REMARK)

1. Label Specifications :

MODEL:
LOT NO:
QUANTITY:
CHECK:

2. 靜電袋上不貼膠帶

3.放置時LCD面同朝前方放置

POWERTIP
JAN 23 2008
R&D APPROVED

JP-R-382-01